ESD-TDR-63-128

SOLID STATE TACAN RECEIVER/CODER

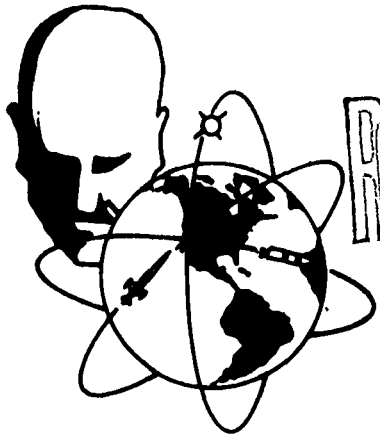
INTERIM SCIENTIFIC REPORT

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-63-128

MARCH 1963

N. R. Ascione
J. C. Cozzie
R. E. Torregrossa

482L/431L SYSTEMS PROGRAM OFFICE
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts



SYSTEM 482L

(Prepared under Contract No. AF 19(604)-8352 by the Ground Systems Lab., ITT Federal Laboratories, 500 Washington Avenue, Nutley 10, New Jersey)

ESD-TDR-63-128

SOLID STATE TACAN RECEIVER/CODER

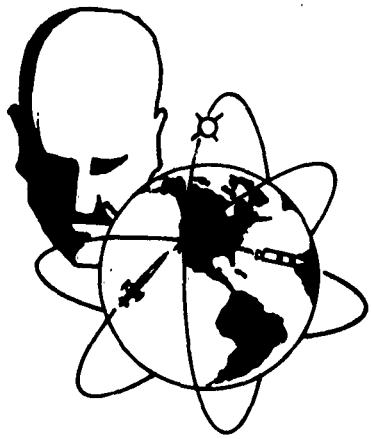
INTERIM SCIENTIFIC REPORT

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-63-128

MARCH 1963

N. R. Ascione
J. C. Cozzie
R. E. Torregrossa

482L/431L SYSTEMS PROGRAM OFFICE
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
L. G. Hanscom Field, Bedford, Massachusetts



SYSTEM 482L

(Prepared under Contract No. AF 19(604)-8352 by the Ground Systems Lab., ITT Federal Laboratories, 500 Washington Avenue, Nutley 10, New Jersey)

Solid State TACAN Receiver Coder

Prepared by

N. R. Ascione - Project Engineer

R. E. Torregrossa - Engineer

J. C. Cozzie - Junior Engineer

Reviewed by

F. L. Fielding - Senior Project Engineer

Approved by

D. T. Latimer - Laboratory Director

Ground Systems Laboratory
ITT Federal Laboratories
500 Washington Avenue
Nutley 10, N. J.

"THIS ABSTRACT IS UNCLASSIFIED"

ABSTRACT

The initial design of a receiver-coder for use as part of a solid-state TACAN transponder is discussed. Techniques developed for specific problem areas are covered, and experimental results obtained from a 'breadboard' model given.

The possible implications of the program on future TACAN development are examined and recommendations made for the future course of development.

This Technical Documentary Report has been reviewed and is approved. However, publication of this report does not constitute Air Force approval of the recommendations in Section 11.

J. E. REEGAN
Technical Contract Monitor

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

1.1 The initial contract under which the work described in this report was performed was awarded 18th February, 1961, and required essentially the design and development of a 'breadboard' model of a solid-state TACAN receiver-coder and an operating temperature test at the extremes of both 0°C and +70°C (adjusted at +32°C), and 0°C and -40°C (adjusted at -15°C). On 1st March, 1962, the original contract was extended both in time and work content to include the development of additional transponder circuitry, particularly in the receiver-coder, and an evaluation of the GE ZP1022 tetrode. The add-on also required the incorporation of the developed circuitry in a GFE AN/TRN-17 in order to permit comparison between the equivalent solid-state and tube units.

1.2 This interim scientific report covers the initial development phase and some temperature testing of the receiver-coder proper.

SECTION 2

SYSTEM CONSIDERATIONS

2.1 The solid-state Receiver-Coder discussed in this report has been divided into several modules according to function and as an aid in testing and packaging. The interconnection of the modules is shown in Figure 1, a brief functional description appearing below. It will be noted that "DME only" operation may be obtained by deleting the north and auxiliary burst generators.

a) IF Amplifier - consists of ten double-tuned stages, a video amplifier and a ferris discriminator, the latter providing the adjacent channel rejection.

b) Decoder and Spike Eliminator - rejects interrogations that are not properly coded, and pulses whose widths do not exceed a specified minimum regardless of coding.

c) Identity - generates identity coded pulses from the 1350 cps antenna tone wheel and establishes priority between the identity and squitter pulses as directed by the keyer.

d) Internal Noise Source and Internal AGC - injects internally generated noise into the decoder when the i-f squitter rate drops below 2700 pulses per second, the amount of injected noise being controlled by the Internal AGC circuit which counts the decoder squitter output.

e) IF Amplifier AGC - counts the decoder squitter output and adjusts the i-f amplifier gain so as to maintain an output pulse rate of 2700 pulses per second.

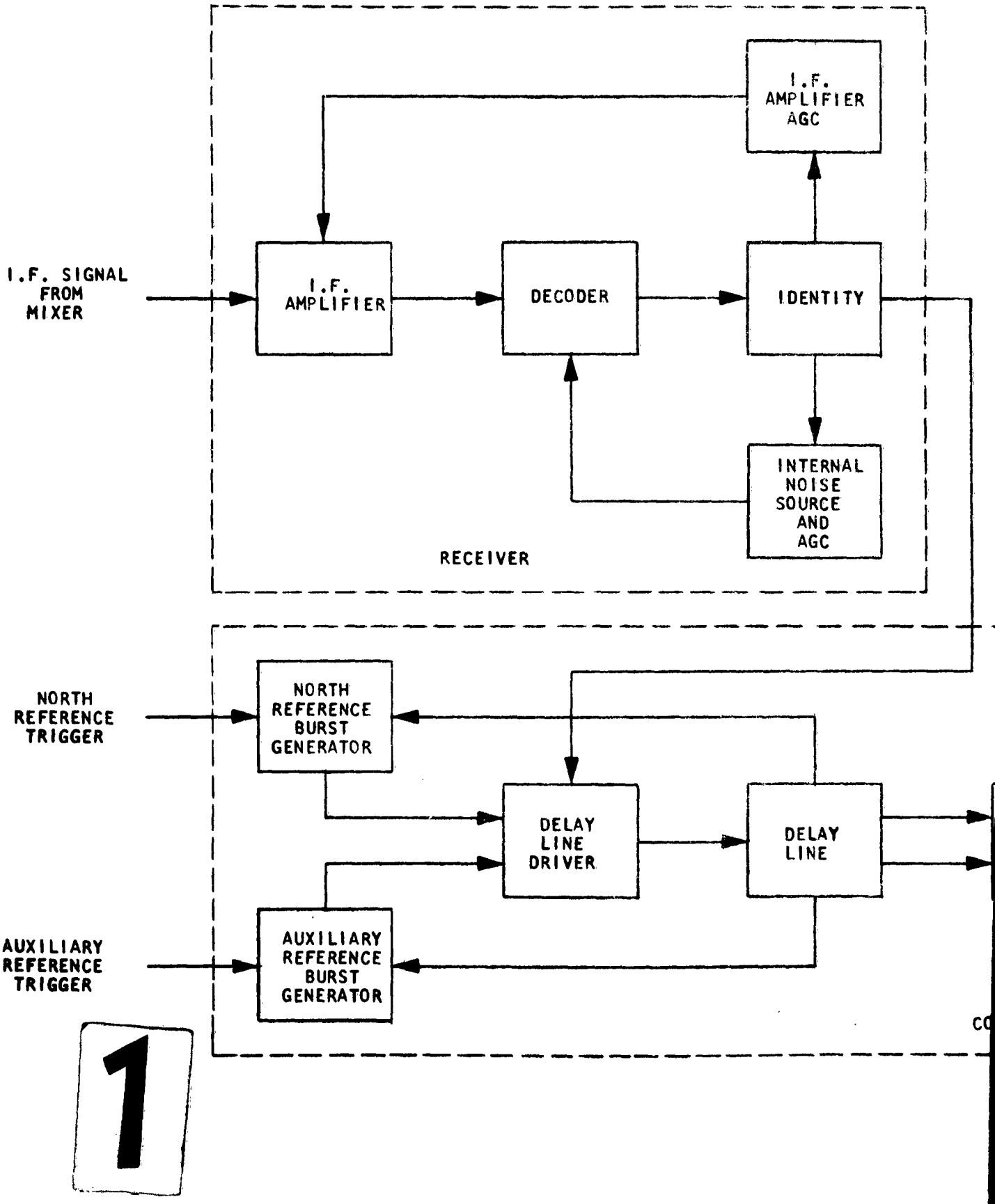
f) North Reference Burst Generator - generates the North Reference Burst and North Precedence Gate from the north antenna trigger.

g) Auxiliary Reference Burst Generator - generates the auxiliary reference burst and auxiliary precedence gate from the auxiliary antenna trigger.

h) Delay Line Driver - processes the reference marker bursts, assigning them priority over the identity/squitter signal obtained from the identity module.

i) Timing - sets the overall beacon delay, provides the pulse pair coding and generates a blanking waveform for disabling the receiver during transmission.

j) Shaper - shapes the video pulses applied to the modulator in order to minimize the energy transmitted on the adjacent channel.


I.F. AMPLIFIER AGC
I.F. SIGNAL FROM MIXER
I.F. AMPLIFIER
DECODER
IDENTITY
INTERNAL NOISE SOURCE AND AGC
RECEIVER
NORTH REFERENCE TRIGGER
NORTH REFERENCE BURST GENERATOR
DELAY LINE DRIVER
DELAY LINE
AUXILIARY REFERENCE TRIGGER
AUXILIARY REFERENCE BURST GENERATOR
CO

1

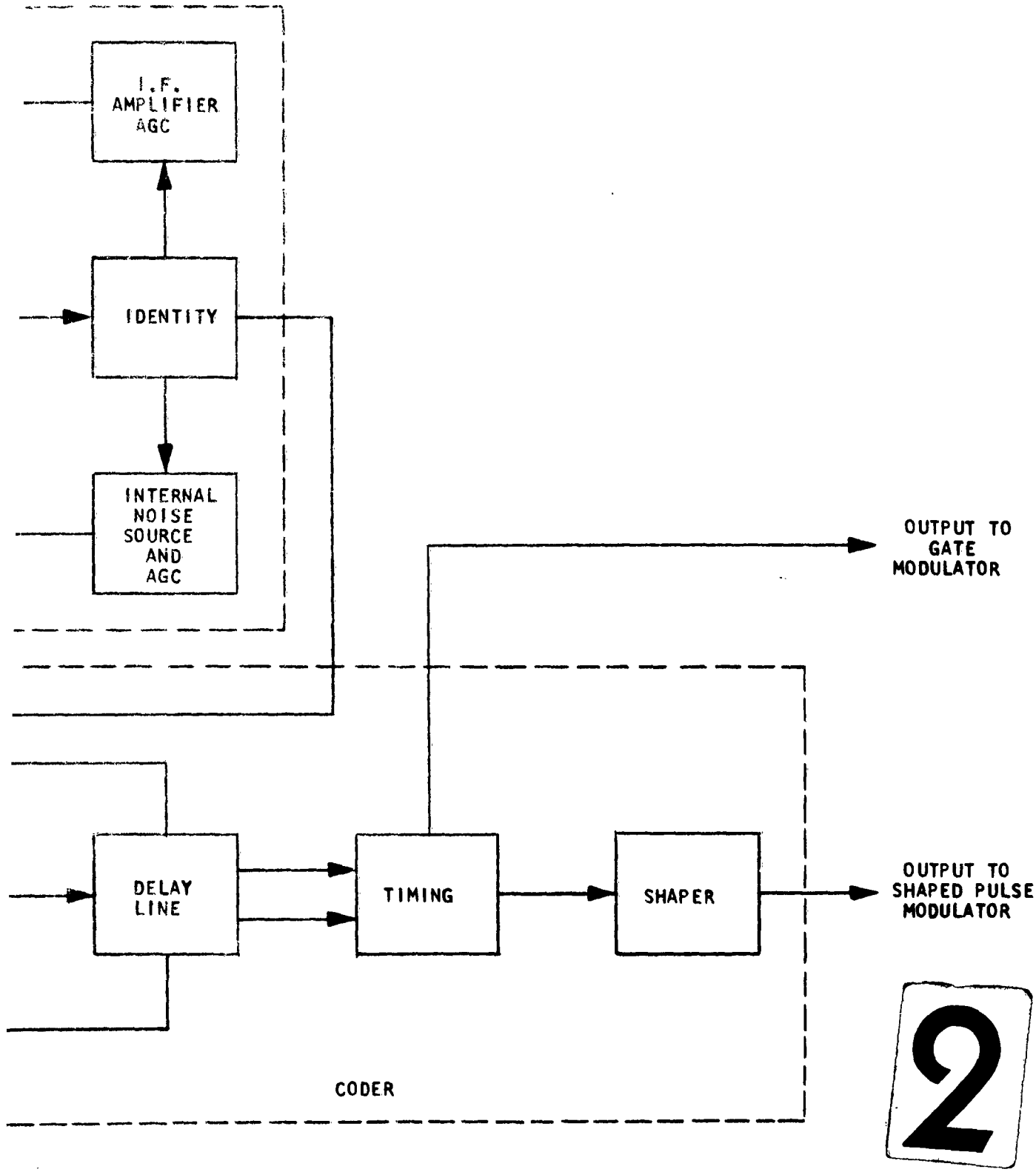


FIGURE 1
RECEIVER CODER BLOCK DIAGRAM

SECTION 3

I.F. AMPLIFIER

3.1 The IF Amplifier design is based on the specifications listed in Table 1.

TABLE 1

Center Frequency	63 Mc
Bandwidth at 3db points	3 Mc
Gain	120 db
AGC Range (minimum)	65 db

Initial evaluation was performed on a three stage breadboard, and from it a complete IF strip with Ferris discriminator was constructed.

3.2 The choice of transistor type in a high frequency amplifier is of maximum importance and is concentrated in two major areas; frequency stability and parameter variation with operating point. Internal feedback inherent in all transistors causes them to be bilateral in nature and may result in instability at certain frequencies. Pritchard (1) has derived an expression for a critical frequency ω crit. (Equation 1) above which a transistor employed in the common emitter configuration may be unconditionally stable.

EQUATION 1

$$\omega_{crit} = \frac{0.4\gamma_{e'}\omega\alpha_b}{\gamma_{b'}}$$

Hence, a transistor whose properties are such that ω_{crit} does not exceed the lowest operating frequency must be selected.

3.3 It is a well known fact that the small signal parameters of a transistor vary with operating point. These parameters can alter the shape of the frequency response, since they along with any external components employed, determine the Q and resonant frequency of the interstage bandpass filters. Accordingly, the usual methods of applying AGC by varying the DC operating point, i.e. varying Vc or I_E, cannot be employed without further compensation.

3.4 As a result of these stability and AGC considerations, the 3N35 silicon tetrode transistor was chosen. This unit, while exhibiting unconditional stability above 50MC and excellent high-temperature characteristics, affords dual element control for AGC application. By varying both I_E and I_{B2}, the input and output parameter variations can be made to compensate for each other thus maintaining a flat bandpass response.

3.5 For relative ease of tuning and component uniformity, synchronously tuned, inductively coupled doubles are used in the interstage circuits. Transitional coupling is employed in order to attain a flat topped response, and maximum power transfer is obtained by making the primary and secondary Q's equal, thereby, coupling critically as well as transitionally.

3.6 Impedance mismatch is necessitated in order to minimize the adverse effects of internal feedback inherent in the transistors, and provide easier tuning. While sacrificing some power gain the mismatch technique does tend to reduce the effect of parameter variation between production batch units of transistors.

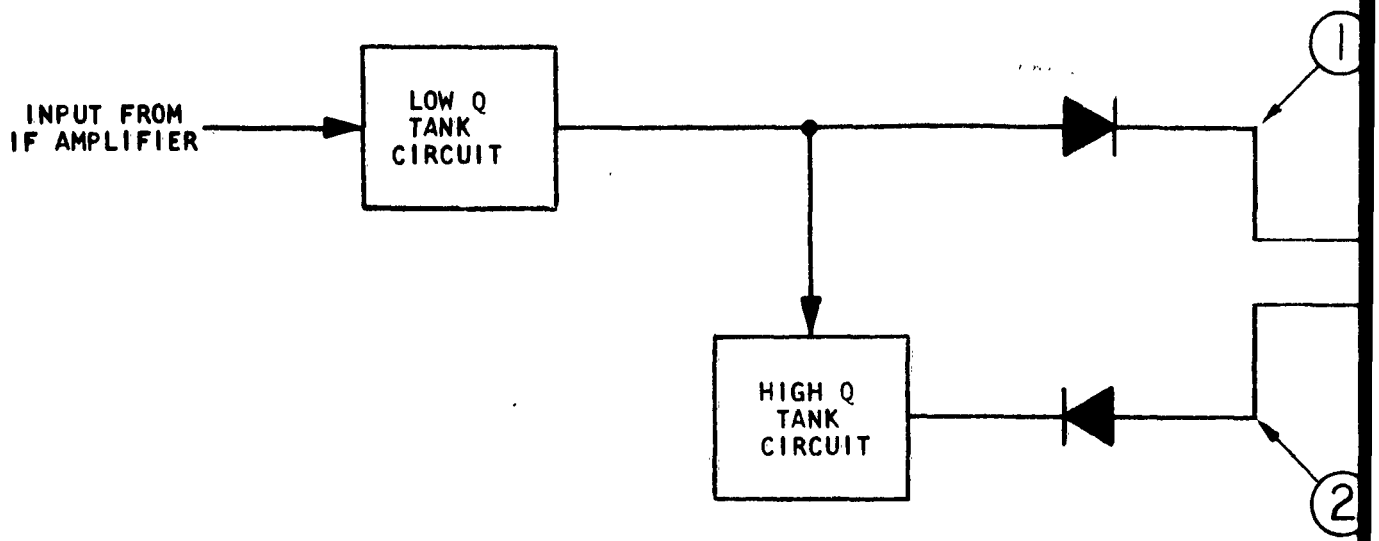
3.7 High selectivity of the wanted channel is achieved in the Ferris discriminator by using two tuned circuits of different Q's, each tuned to the same frequency, and each connected to a diode rectifier giving signals of opposite polarity. These two circuits individually produce selectivity curves as shown in Figure 2. When these outputs are combined, the signals on the wanted channel are negative going when rectified and those on the adjacent channel positive going, so providing sharp rejection of all adjacent channel energy. (Subsequent stages accept unidirectional inputs corresponding to the "on" channel only.)

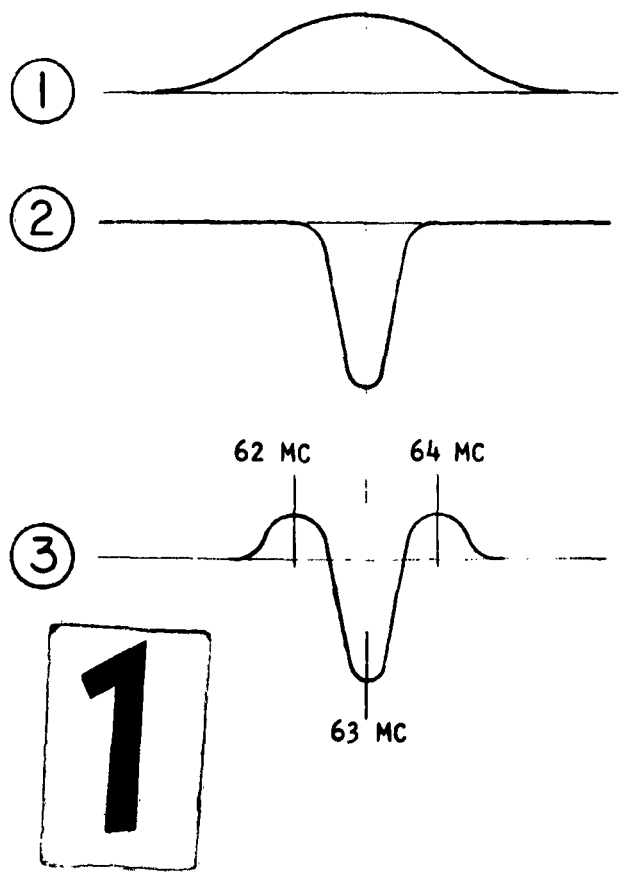
3.8 The main area of difficulty during the program has been the lack of interchangeability of transistors. The spread in impedance parameters from unit to unit was too significant to be cancelled through mismatch techniques alone. Extensive tests, measuring parallel input and output impedances R_{iep}, C_{iep}, R_{oep}, and C_{oep}, were performed on twenty randomly selected Texas Instrument Corporation 3N35 tetrodes. These measurements, taken on a Boonton RX meter, were the prime subject of repeated correspondence with Texas Instrument. At the date of this report the status of this correspondence is as follows:

a) Five of the 3N35 units tested at ITTFL were forwarded to the manufacturer for verification of the test data.

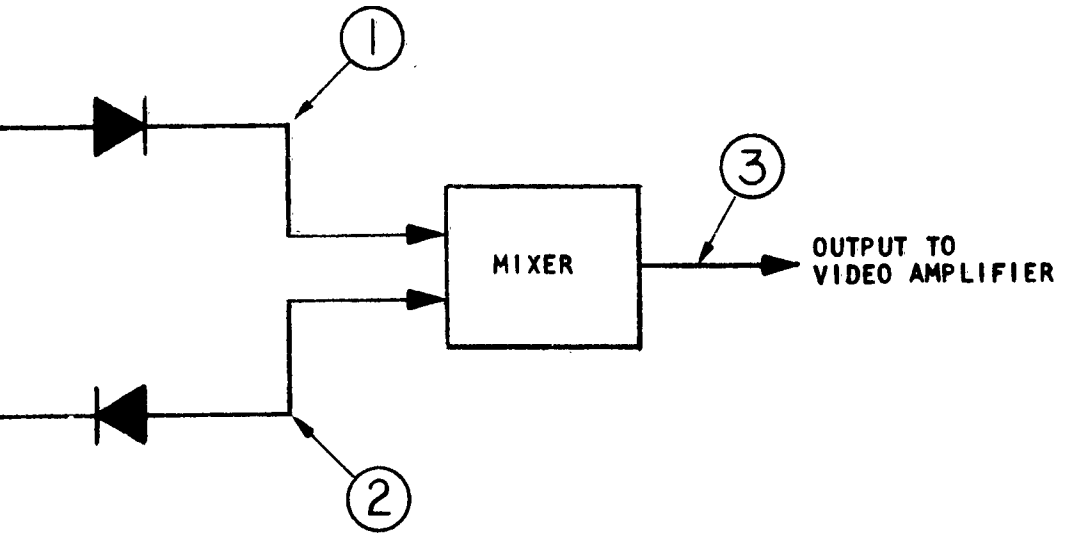
b) Ten 3N35 units, meeting JAN requirements, were sent to ITTFL by Texas Instruments for test sample use. The JAN units, priced 10% higher than the standard 3N35, were reputed to have more uniformity. When tested by ITTFL they exhibited a closer relationship to each other, however, mean values deviated from the manufacturer's suggested design values.

c) A tentative appointment to visit ITTFL in February, 1963, was made by Texas Instruments' Texas office. It is hoped that this meeting will resolve the problem of having to hand select transistors.

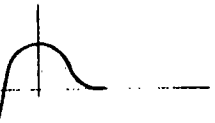

INPUT FROM
IF AMPLIFIER
LOW Q
TANK
CIRCUIT
HIGH Q
TANK
CIRCUIT
1
2


1
2
3
62 MC
64 MC
63 MC

1



64 MC



C

2

FIGURE 2
FERRIS DISCRIMINATOR

3.9 The effects of AGC control on bandwidth and center frequency were investigated on a three stage breadboard. From Figure 3, it can be seen that the center frequency shifted 1.8 MC and the 3db bandwidth shrunk 1 MC as the amplifier was put through 40db of gain reduction, indicating that the input and output parameter variations were not exactly compensating for each other.

3.10 These changes in center frequency and bandwidth could be tolerated if a separate passive bandpass filter were employed in conjunction with a wideband IF Amplifier. The bandpass response would then be determined solely by the filter, and bandwidth shrinkage could take place without disturbing the composite filter-amplifier response, provided the amplifier bandpass is never less than that of the filter. Center frequency shift in the amplifier would be meaningless as long as its response curve remained flat.

3.11 The deliverable IF Amplifier assembly, Figure 4, consists of ten stages of intermediate frequency amplification followed by a Ferris frequency discriminator and one stage of video amplification.

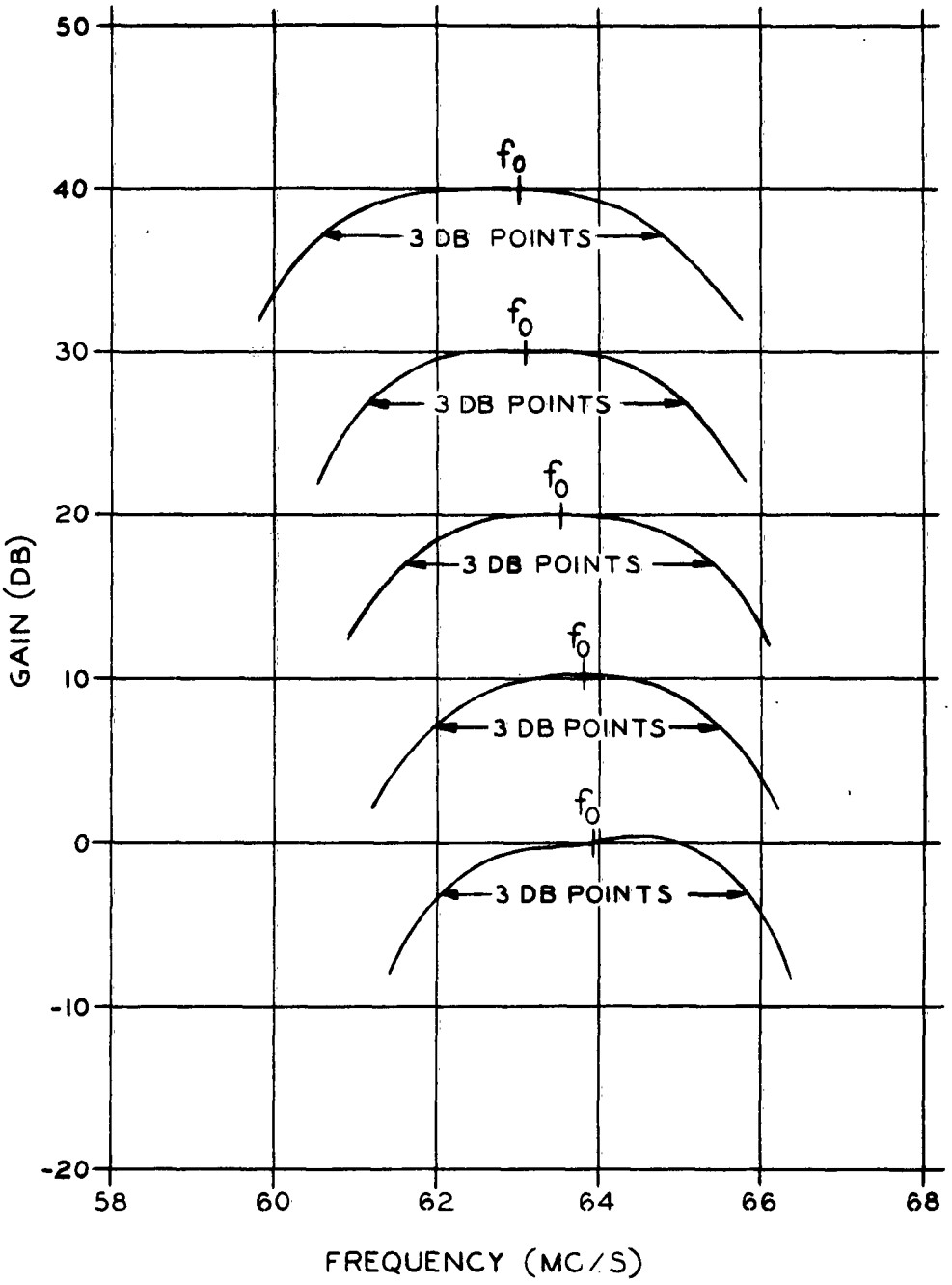
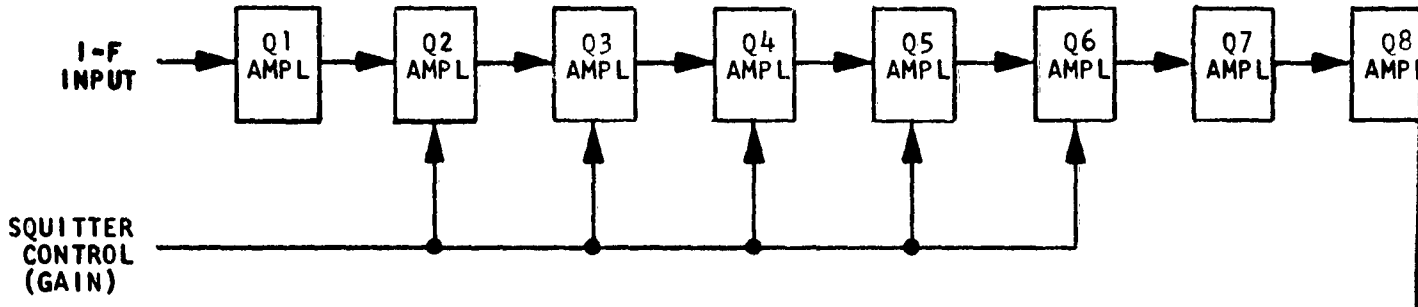
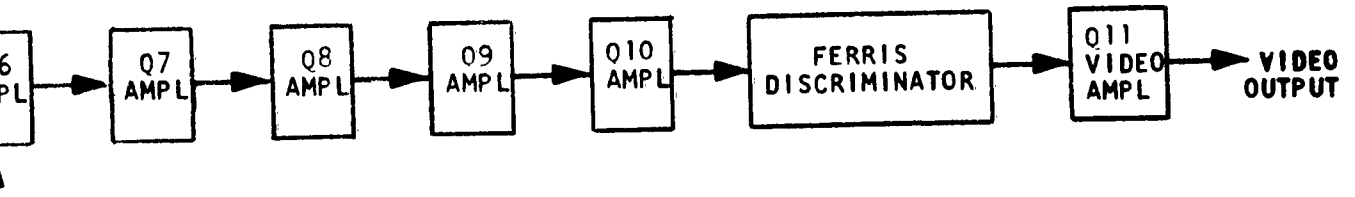


FIGURE 3
AGC CHARACTERISTICS OF 3 STAGES OF 3N35-63 MC S.S. IF STRIP


I-F
INPUT
Q1
AMPL
Q2
AMPL
Q3
AMPL
Q4
AMPL
Q5
AMPL
Q6
AMPL
Q7
AMPL
Q8
AMP
SQUITTER
CONTROL
(GAIN)

1



2

FIGURE 4
AMPLIFIER I.F.

SECTION 4

DECODER AND SPIKE ELIMINATOR (See Fig.5)

4.1 The rejection of pulses of widths 1 μsecond or less is accomplished in the IF Amplifier Ferris discriminator by means of an inhibiting pulse derived in the decoder. The Ferris discriminator is the only suitable point for spike elimination since its primary is the last point in the receiver with the bandwidth necessary for preserving the shape of narrow pulses. As the video bandwidth at the Ferris secondary is only 200 kc, a 1 μsecond input pulse would be stretched so that its half-amplitude width was 1.2 μseconds, the trailing edge persisting for 2.76 μseconds after the initiation of the pulse. The Ferris primary, however, with its 1.5 megacycle video bandwidth reproduces a 1 μsecond pulse with good fidelity, the width remaining at 1.0 μseconds and the trailing edge only 0.22 μseconds.

4.2 Basically then, the i-f signal is sampled at the Ferris primary, amplified and impressed upon a delay line whose output is shorted. This generates an inhibit pulse the width of which is equal to that of the input pulse for pulses of width less than the two-way delay of the shorted line, and equal to the two-way delay for the case where the input pulse width exceeds the two-way delay. This inhibit pulse is used to forward bias a diode shunting the Ferris secondary to ground. Thus, should the width of the incoming pulse be equal to or less than the two-way delay of the line, there will be no output from the Ferris secondary. For an input pulse whose width T1 is greater than twice the line delay, T_D, an output pulse width of $(T1 - 2T_D)$ will be realized. Decoding, therefore, will occur not on the leading edge of the interrogation pulse, but $2T_D$ μseconds later. If the beacon delay is not to shift with variations in temperature and input level, it is imperative that the delay introduced by the spike eliminator be independent of these parameters. Since an IF Amplifier was not available for test at the time the spike eliminator was developed, data was compiled with a pulse amplifier simulating the Ferris secondary. Tests were performed on the spike eliminator with an input pulse width of 3 μseconds. The time delay from the leading edge of the interrogation pulse to the half-amplitude point of the leading edge of the output pulse was monitored as both temperature and input amplitude were varied. The results are tabulated below.

IDENTITY KEYER

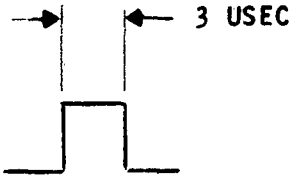
I.F. AMPLIFIER DETECTOR OUTPUT

NOISE GENERATOR OUTPUT

VIDEO AMPLIFIER

BLANKING & DEADTIME PULSE FROM IDENTITY MODULE

DECODER OUTPUT TO IDENTITY MODULE



OUTPUT FROM FERRIS DISCRIMINATOR PRIMARY

AMPLIFIER

INHIBIT PULSE TO FERRIS DISCRIMINATOR SECONDARY

1

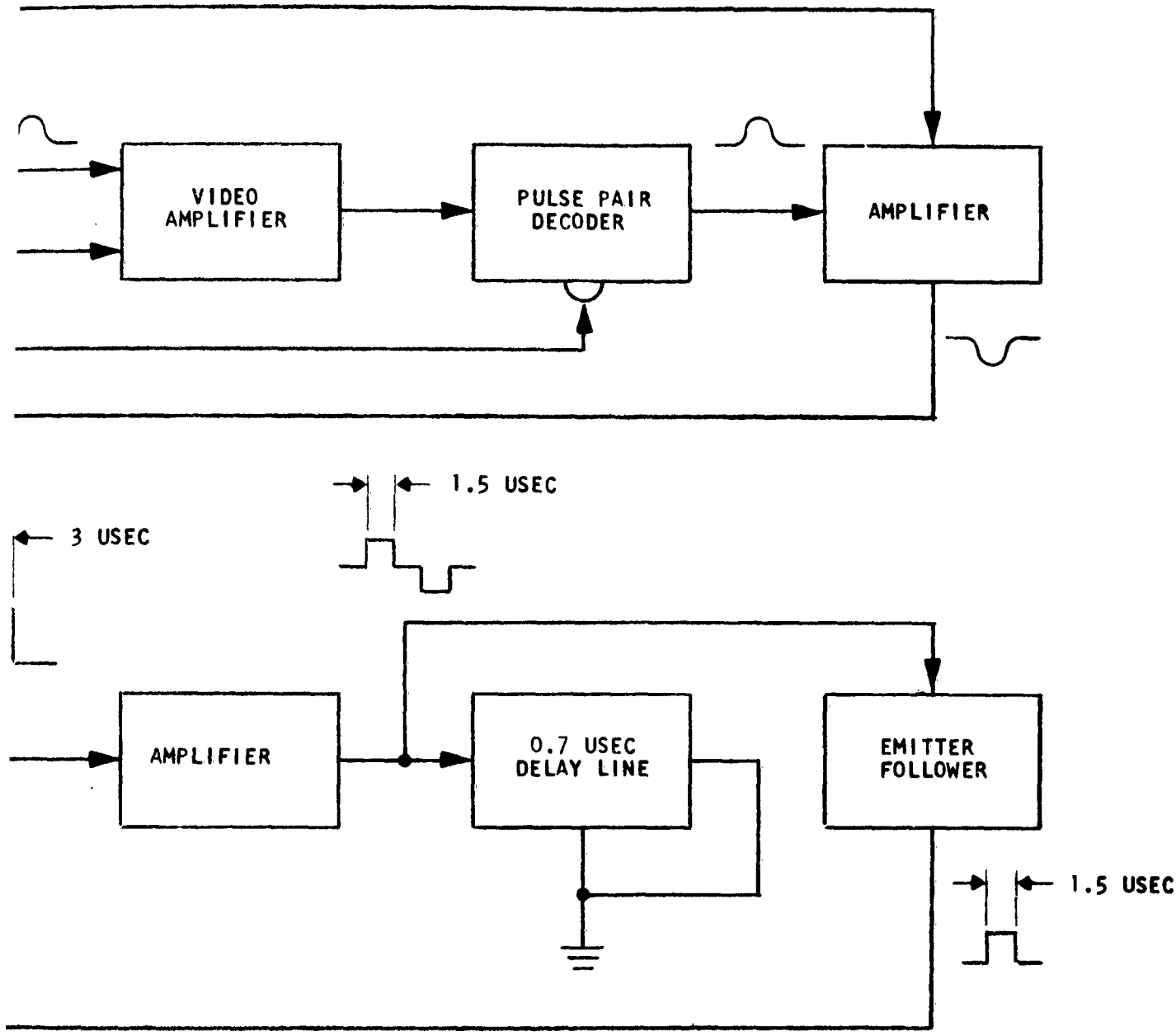


FIGURE 5
DECODER MODULE

TABLE 2

T Maintained at +25°C

Pulse Amplitude in Volts	Delay Microseconds	Change in Delay in Microseconds
0.5	1.65	0
1.0	1.65	0
1.5	1.64	-.01
2.0	1.64	-.01
2.5	1.62	-.03

TABLE 3

Pulse Amplitude Maintained at 1.0 Volts

Temperature	Delay in Microseconds	Change in Delay in Microseconds
+25°C	1.64	0
-40	1.65	-.01
+80	1.64	0

4.3 The pulse pair decoder consists of a delay line controlled coincidence circuit and a video amplifier. In the latter, emitter-to-base feedback is employed over two stages in an effort to stabilize the gain and make it relatively independent of variations in transistor parameters with temperature and between units. A derivation of the gain expression for the feedback-amplifier-pair appears in appendix no. 2.

4.4 It may be seen that if high gain low leakage transistors, such as the 2N338, are used, the overall gain is determined by the external circuit only and is given by $K = \frac{R_e + R_f}{R_e} \frac{R_L}{R_g}$ *

4.5 The operation of the decoder was checked at room ambient and found to be satisfactory. Complete rejection of improperly coded interrogations was obtained for pulse spacings less than 9.5 μseconds and more than 15.6 μseconds. (The interrogation pulses were 3.5 μseconds wide at the 50% amplitude.)

* K = voltage gain
R_e = emitter resistance
R_f = feedback resistance
R_g = source impedance
R_L = load resistance

SECTION 5

IDENTITY

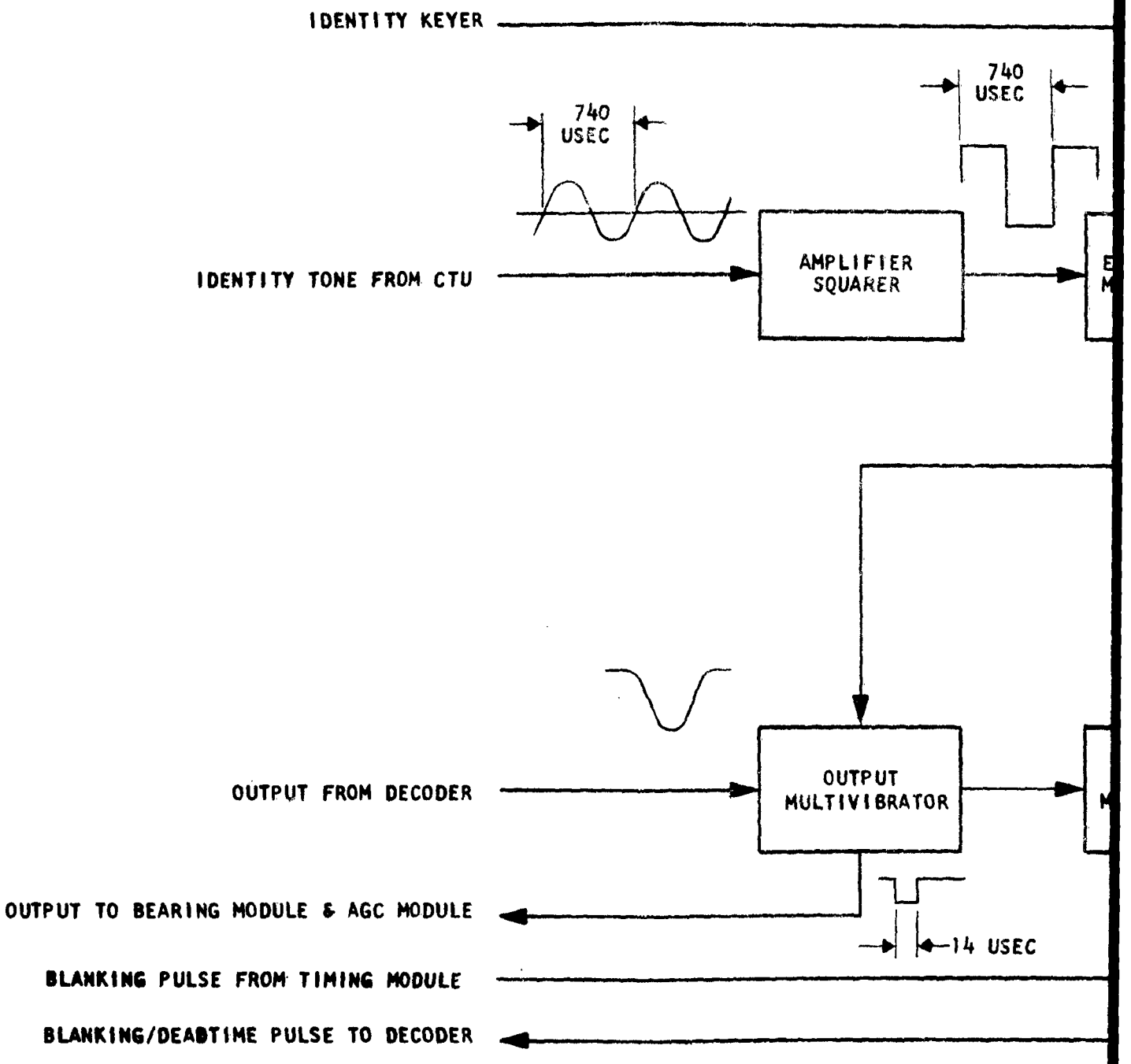
5.1 As may be seen from Figure 6, the identity module is comprised of the identity tone generation circuits, the receiver video output multivibrator and the dead time/blanking generator.

5.2 The antenna tone, a 1350 cycle sinusoid, is shaped by two overdriven amplifiers, where symmetrical clipping and squaring take place. The output of the second amplifier, essentially a 1350 cycle square wave, is used to trigger the identity tone equalization multivibrator, a conventional collector-base coupled monostable multivibrator which generates a 100 μsecond pulse for each cycle of the square wave. Differentiated outputs are taken from each of the multivibrator collectors and used to trigger the output multivibrator during identity tone transmission. During this period, the Identity Keyer provides an enabling signal to the differentiator and disables the output stage of the decoder.

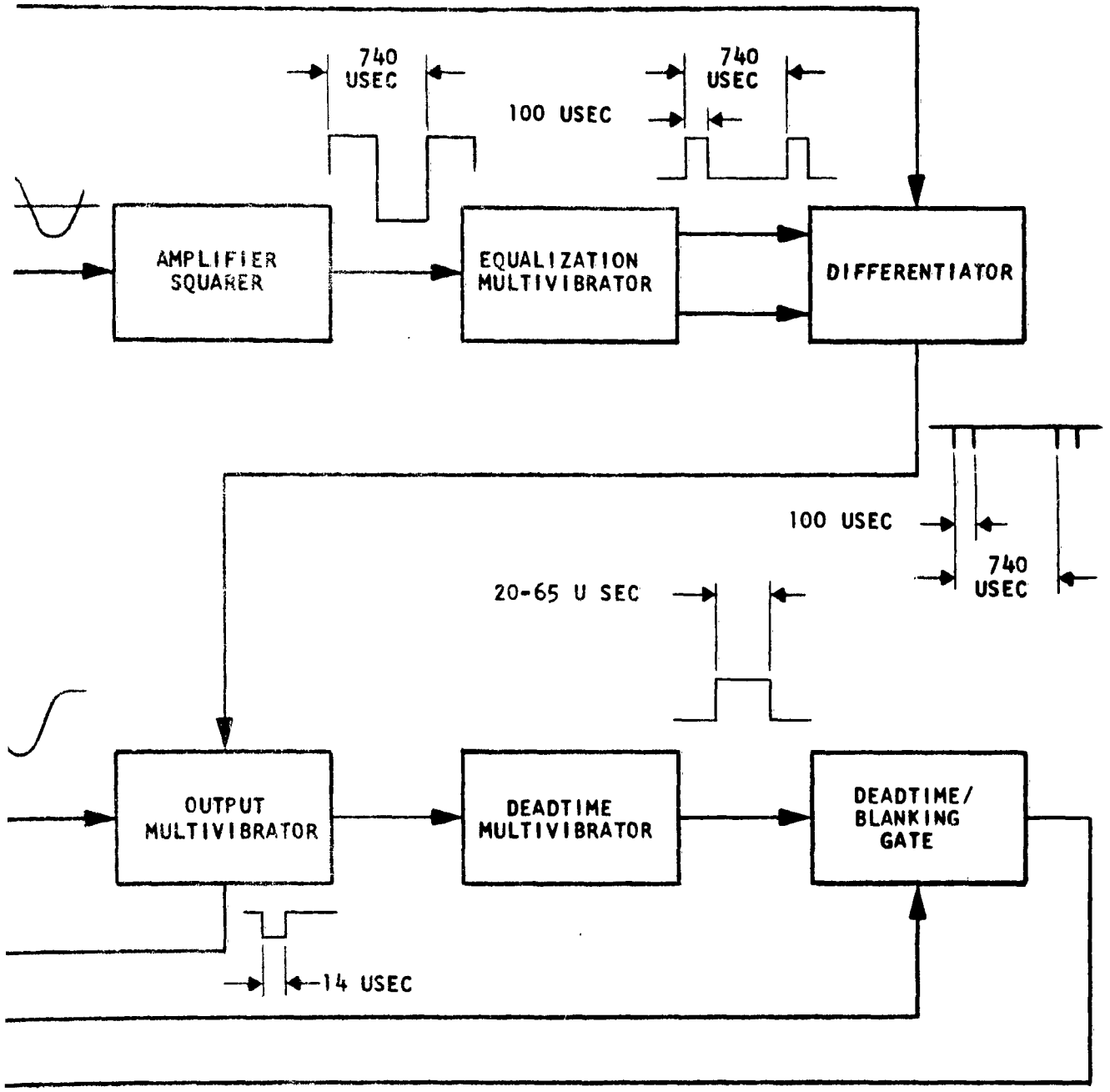
5.3 The output multivibrator, a 14 μsecond collector coupled multivibrator, provides the receiver output signal to the bearing module and also drives the pulse counting circuits in the AGC modules. It is therefore imperative that the timing of this multivibrator be both accurate and independent of transistor parameter variations. This is accomplished by returning the timing resistor to the collector supply, V_{cc}, grounding the collectors, and returning the emitters to the negative supply, V_{ee}, thus utilizing the linear portion of the timing exponential.

5.4 The dead time multivibrator is triggered from the output multivibrator and also employs a collector coupled configuration. Here the wide adjustment range, (20 to 65 μseconds pulse width) obviates the use of a variable resistor in the base circuit of the normally on transistor. Timing is accomplished by a-c coupling the timing resistor into the base circuit. Thus the multivibrator may be adjusted through its range without affecting the d-c operating point.

5.5 The dead time signal is combined with the blanking signal generated in the timing module, and used to disable the decoder.


IDENTITY KEYER
740 USEC
740 USEC
IDENTITY TONE FROM CTU
AMPLIFIER SQUARER
OUTPUT FROM DECODER
OUTPUT MULTIVIBRATOR
OUTPUT TO BEARING MODULE & AGC MODULE
14 USEC
BLANKING PULSE FROM TIMING MODULE
BLANKING/DEADTIME PULSE TO DECODER

1



2

FIGURE 6
IDENTITY MODULE

SECTION 6

INTERNAL NOISE SOURCE AND INTERNAL AGC CIRCUIT

6.1 During the presence of a CW jamming signal, squitter pulses (randomly decoded noise) from the internal noise source are automatically inserted in the decoder. The internal noise AGC circuit counts the squitter output from the identity output multivibrator and generates a d-c control voltage which serves to maintain the squitter rate at 2700 pps. (A block diagram of this module appears in Figure 7).

6.2 The rectangular pulses obtained from the identity output multivibrator, all of equal width and amplitude, are amplified and impressed upon a low-pass RC filter whose output, a d-c signal, is applied as a control voltage to the bias controlled attenuator located in the internal noise source.

6.3 The pulse amplifier, a conventional common-emitter stage, employs a collector-base diode clamp in order to minimize storage time effects over the temperature range. Operation of the pulse amplifier both with and without the diode clamp is summarized in the table below.

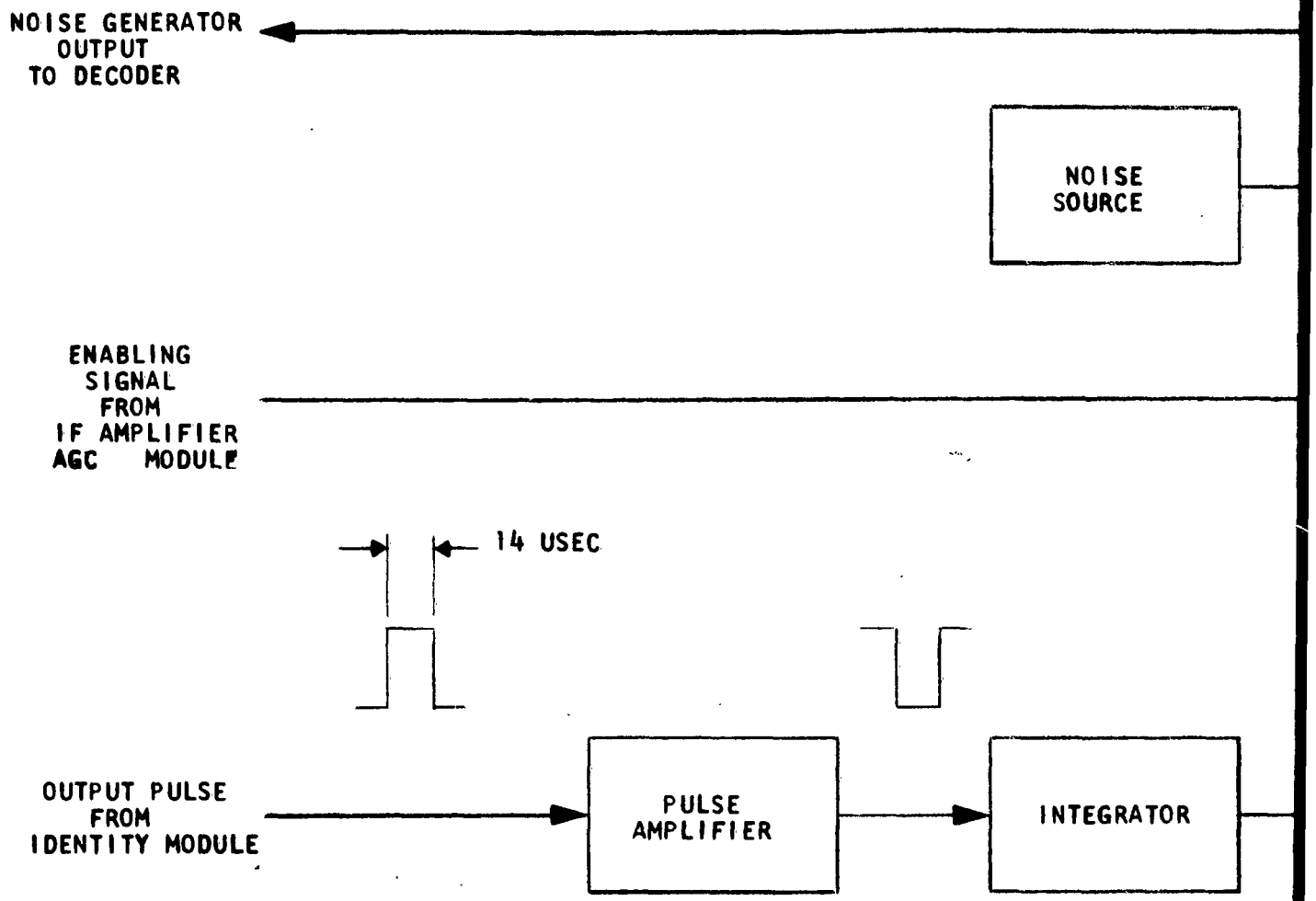
TABLE 4

Temperature °C	Without Diode Clamp			With Diode Clamp		
	Pulse Width μsecond	Change in PW	Change in PRF	Pulse Width	Change in PW	Change in PRF
+25	15.24	-	-	15.62	-	-
-40	14.88	-0.36	+62	15.52	-0.10	+17
+80	-	-	-	15.66	+0.04	-7

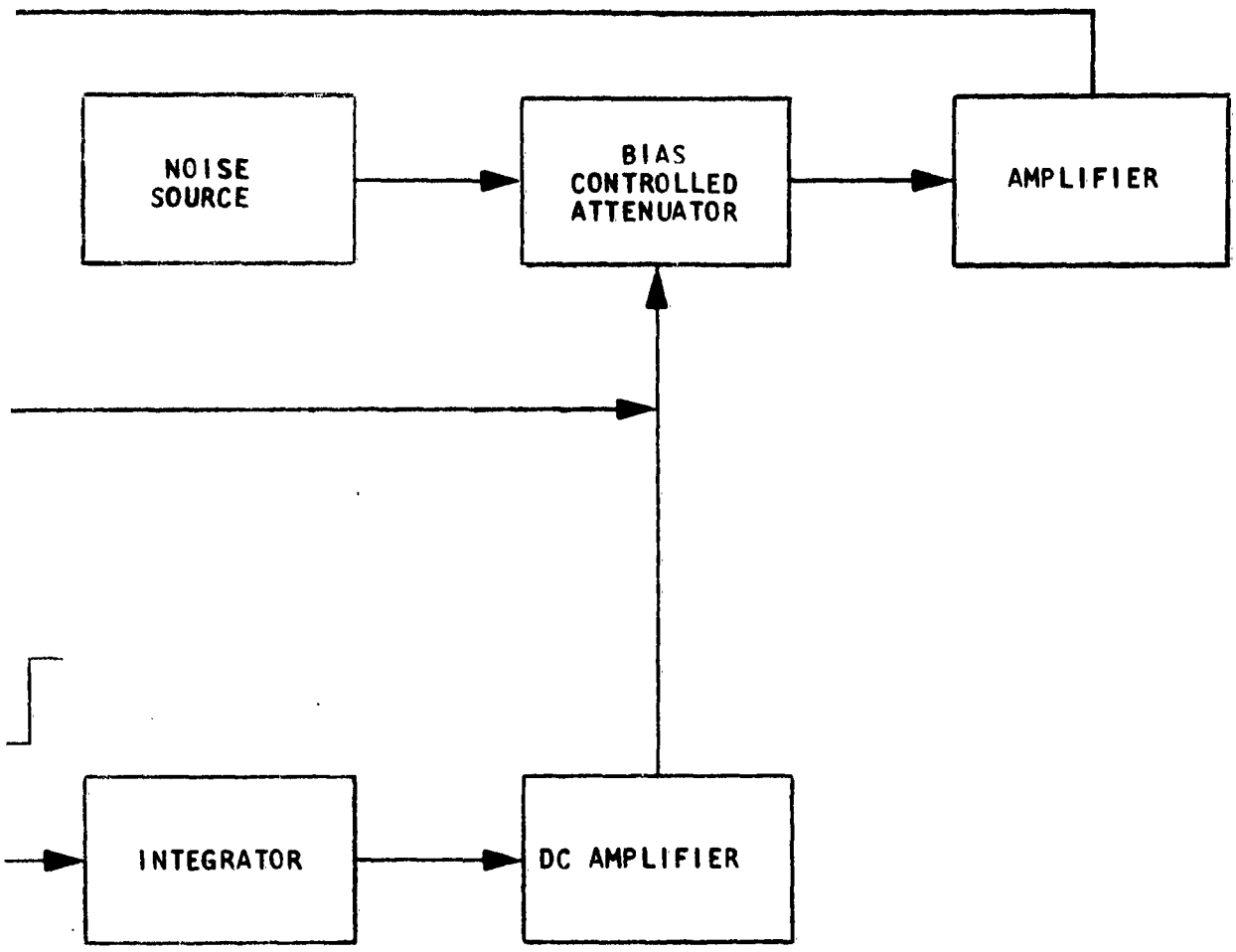
6.4 The factors which effect the operating point and d-c gain of a transistor d-c amplifier are the collector cutoff current, I_{co}, the d-c input conductance, and the d-c common emitter current gain, h_{FE}. Since the transistor is a highly temperature sensitive device, the factors listed above will vary in magnitude over wide ranges as the temperature changes. The use of high quality, low leakage silicon transistors (such as the 2N338) mitigates the effects of changes in I_{co} upon the operating point, while the application of negative feedback techniques stabilize the circuit operation with changes in the d-c current gain. Linear stabilization techniques, however, cannot be utilized to minimize the effects of changes in the d-c input conductance upon the operating point, hence a differential configuration was utilized. Here the change in input conductance, manifested as a change in the base-emitter voltage, V_{be}, is offset by a corresponding change in the base-emitter voltage of the second half of the differential amplifier. The output voltage of the d-c amplifier used in this application is given by the expression

$$e_o = (e_2 - e_1) + (V_{be_2} - V_{be_1}) \frac{R_c}{R_e} *$$

*See Item 5 List of References (V_{be} - base emitter voltage)
(R_d - collector resistance)


NOISE GENERATOR OUTPUT TO DECODER
NOISE SOURCE
ENABLING SIGNAL FROM IF AMPLIFIER AGC MODULE
14 USEC
OUTPUT PULSE FROM IDENTITY MODULE
PULSE AMPLIFIER
INTEGRATOR

1



2

FIGURE 7
INTERNAL NOISE GENERATOR
AND AGC MODULE

The above relation shows that the voltage gain is independent of the d-c current gain and that the change in input conductance is compensated for by the emitter-coupled stage.

6.5 The internal AGC circuits above were subjected to temperature tests and the squitter rate monitored. The results are tabulated below.

TABLE 5

Temperature	Squitter Rate	Change in PRF
+25°C	2705	-
-40	2748	+43
+80	2644	-61

Also contained in this module is the internal noise source, comprised of five cascaded RC coupled video amplifiers and a bias-controlled attenuator. The input stage is purposely designed for a poor noise figure by utilizing a high source impedance and collector voltage and a large collector current. Emitter degeneration is provided in all five stages to stabilize the gain and noise output.

6.6 The noise source alone was temperature tested and the squitter rate again monitored. The results are tabulated below.

TABLE 6

Temperature	Squitter Rate	Change in PRF
+25°C	2696	-
-40	2677	-19
+80	2722	+26

The overall operation of this module is summarized in the table below.

TABLE 7

Temperature	Change in PRF AGC	Change in PRF Noise Source	Change in PRF Overall
-40°C	+43	-19	-24
+80	-61	+26	-35

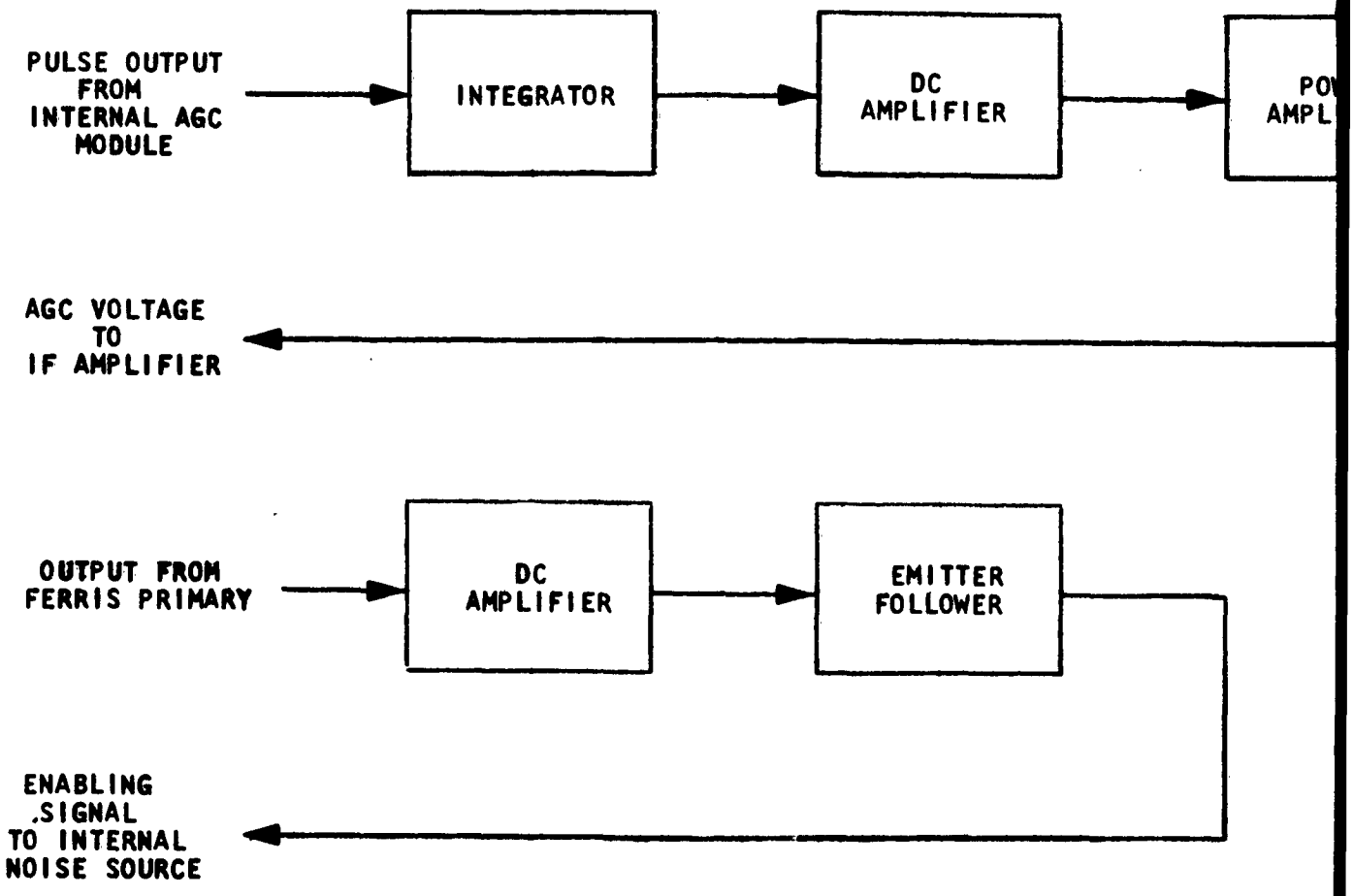
SECTION 7

IF AMPLIFIER AGC CIRCUITS

7.1 Under normal operating conditions squitter is generated from the noise in the output signal of the i-f amplifier. The i-f amplifier AGC circuit maintains the squitter rate at 2700 pps by counting the pulses from identity output multivibrator in a manner similar to that used by the Internal AGC circuit, and subsequently adjusting the i-f amplifier gain to compensate for any change in repetition frequency.

7.2 The same RC low-pass filter and d-c amplifier utilized by the Internal AGC circuit are used here. (See Figure 8). The d-c amplifier, however, is followed by a power amplifier designed for a high input impedance so that it does not load the differential amplifier, a low output impedance, and a highly stabilized gain, so that transistor parameter variations with temperature and between units do not affect the operating point and overall gain.

7.3 This module will also contain the internal noise enabling circuits. Basically, what is required here, is a d-c amplifier which will monitor the d-c level at the Ferris discriminator primary. This voltage is normally at a low level but rises sharply during periods of CW jamming. The increase will be sensed by the d-c amplifier and is used to switch the bias-controlled attenuator, located in the noise source, from an open state into a controlled region of operation.


PULSE OUTPUT FROM INTERNAL AGC MODULE
INTEGRATOR
DC AMPLIFIER
AGC VOLTAGE TO IF AMPLIFIER
OUTPUT FROM FERRIS PRIMARY
DC AMPLIFIER
EMITTER FOLLOWER
ENABLING SIGNAL TO INTERNAL NOISE SOURCE

1

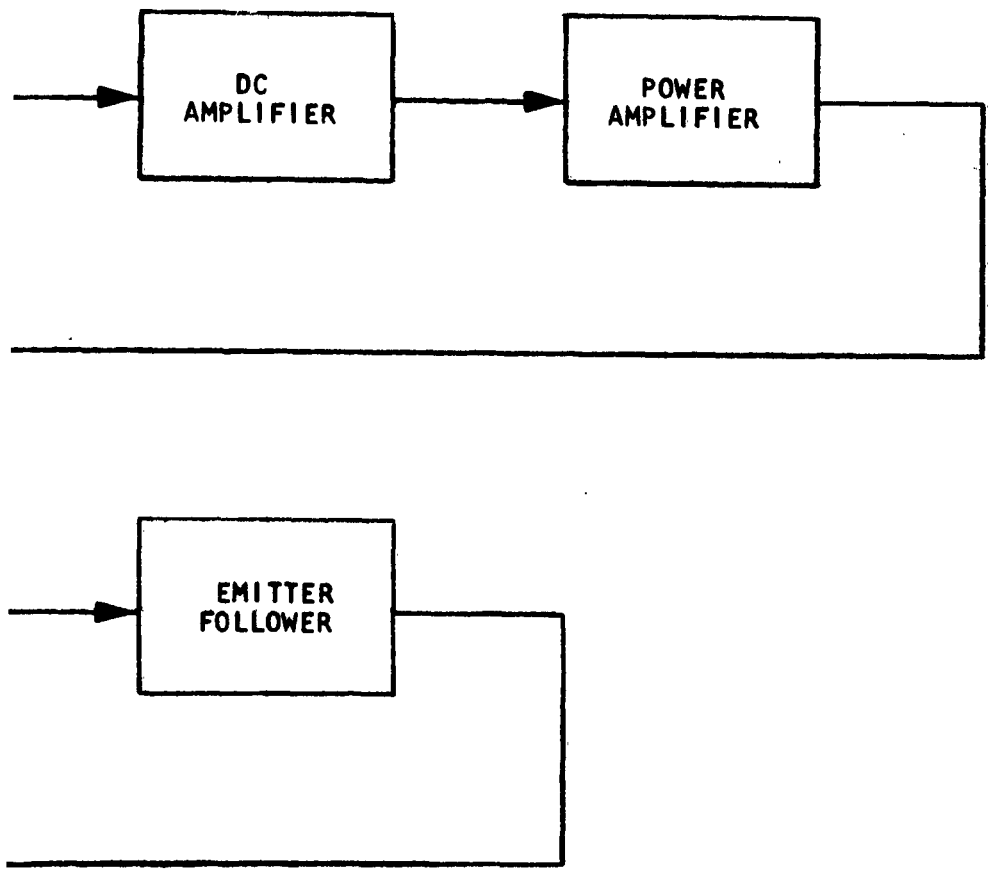


FIGURE 8
IF AMPLIFIER AGC

2

SECTION 8

BEARING MODULE (See Figs. 9, 10, and 11)

8.1 The bearing module produces the north and auxiliary reference bursts when triggered by pulses from the antenna. The encoding of the bearing information into a form suitable for transmission is accomplished by the use of a "ring around" technique, which utilizes a delay line. The advantage of this system is that all the pulse spacings are the same. If a gated oscillator is used, the spacing between the first and second pulses is longer than the spacing of the pulses of the rest of the burst.

8.2 While the trigger pulse from the antenna varies in amplitude and width, its zero cross-over point is consistent, and may be used as the time reference for the position of the antenna. The trigger pulse is fed into a two stage trigger amplifier which clips, amplifies, and differentiates it to yield a negative spike, the leading edge of which coincides within several μs with the zero cross over point of the trigger pulse. The exact zero cross over point could be selected, however, more components would be needed, and the added accuracy is considered unnecessary.

8.3 The trigger amplifier simultaneously fires two multivibrators, a 375 μs (north reference generator), and a 30 μs. The outputs of these multivibrators drive an "INHIBIT" gate whose output, a pulse of 354 μs duration (375 μs - 30 μs), turns on an "AND" gate. (Figure 9). The 30 μs multivibrator output is also differentiated and triggers the delay line driver which in turn feeds a 4 μs pulse into the delay line (Figure 11). After a delay of 30 μs, the pulse is amplified and applied to the "AND" gate which in turn allows the pulse to trigger the delay line driver. This is the beginning of the ring around action, the net result of which is a train of pulses, each 4 μs wide, and spaced 30 μs apart. The gate multivibrator turns the "AND" gate off after the twelfth pulse. Although the burst is only 330 μs wide, the gate multivibrator is adjusted to be 15 μs longer than necessary so that small changes in width do not affect the number of pulses in the train.

8.4 Normally, squitter from the Identity module is applied to the delay line driver. During transmission of bearing information, the gate multivibrator inhibits the squitter for 375 μs (Figure 11), however the delay line must be cleared of squitter pulses prior to the generation of the marker bursts, and it is for this reason that the reference burst is delayed by the 30 μs multivibrator.

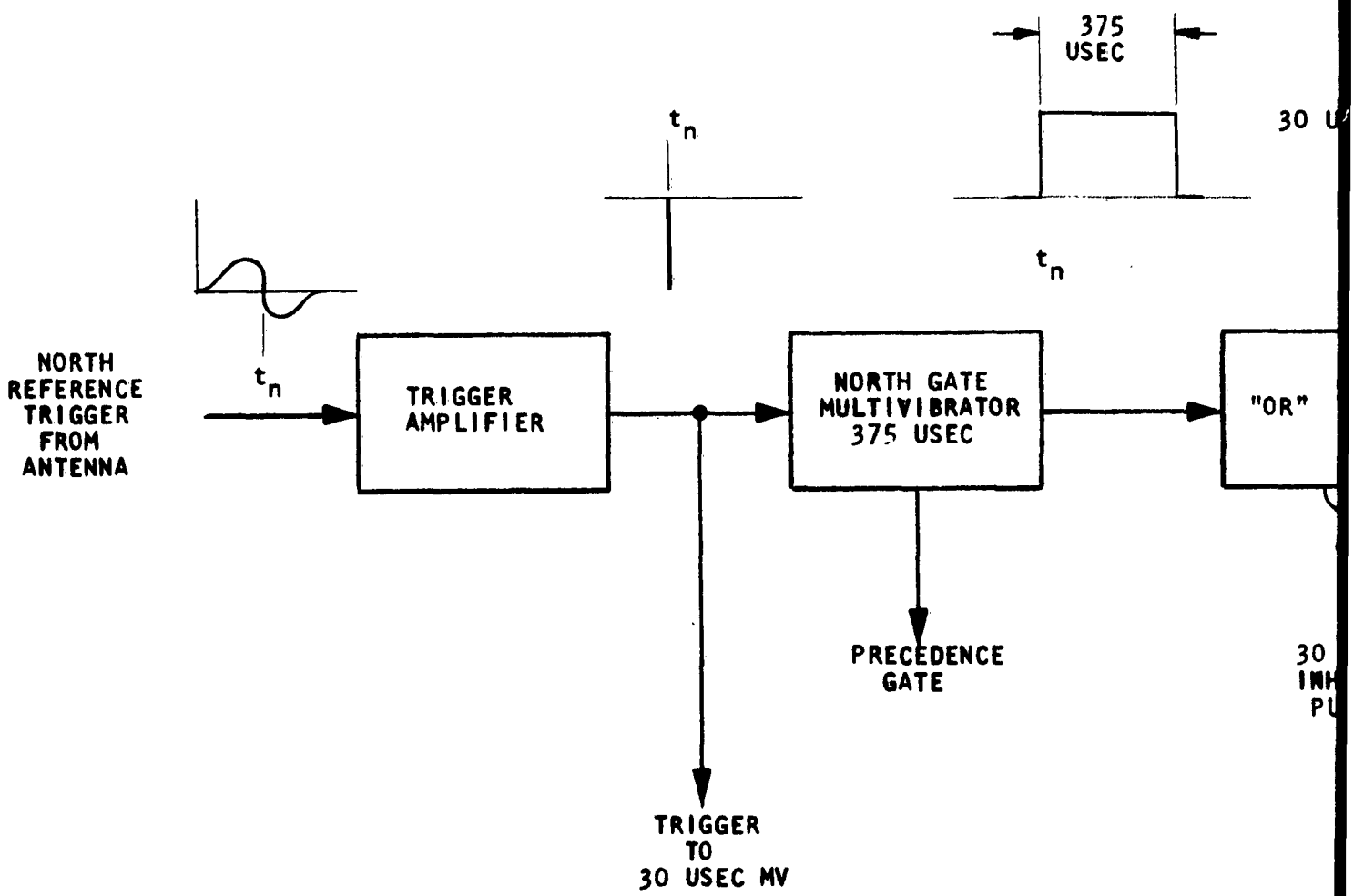
8.5 The auxiliary reference burst is formed in the same manner, (Figure 10) except that the gate multivibrator has a 162 μs pulse width and the pulse spacing is 24 μs.

8.6 The two major temperature problems encountered in the bearing module are the design of a temperature stabilized multivibrator and a ring around circuit in which the change in delay with temperature can be kept to a minimum. The gate multivibrator can be permitted to change a maximum of ±2% over the temperature range so that an RC coupled multivibrator was found to be satisfactory, however, several additions had to be made. A diode was inserted in the base circuit of the normally on transistor to prevent zenering of the base emitter junction because of the 25 volt negative step from the timing capacitor. A diode was also inserted between the timing capacitor and the collector of the normally off transistor, so that a square negative as well as positive pulse can be derived from the multivibrator. This second diode also compensates for changes of voltage drop with temperature across the first diode. The amount of base drive also has a definite influence on temperature stability. The results of tests on a 200 μs multivibrator are given in Table 8 below, together with the delay change, measured by subtracting the pulse spacing at room temperature from the spacing at the temperature extreme.

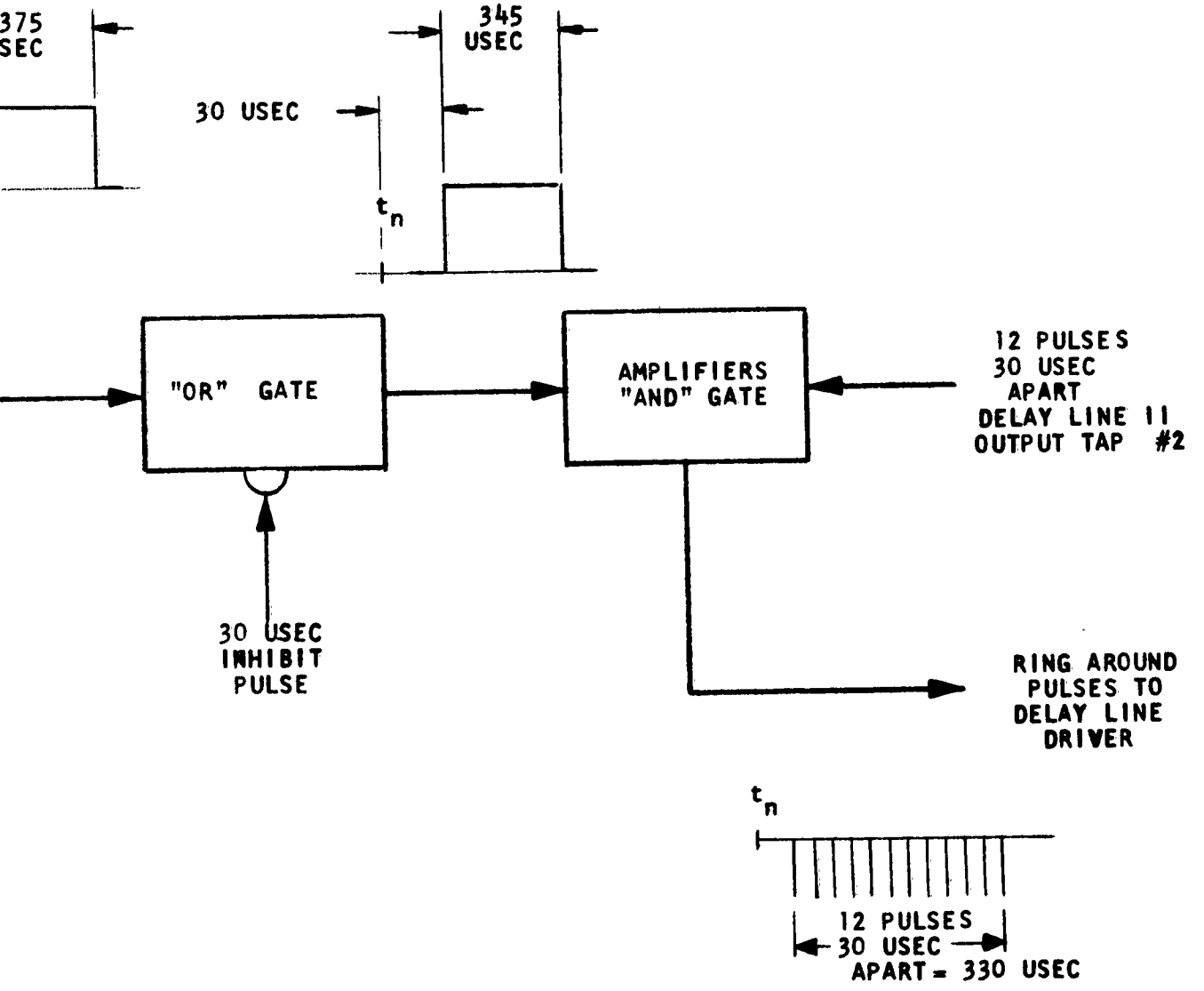
TABLE 8

Temperature °C	Pulse Width of RC Multivibrator	Circuit Delay in ring around
-40	203 μs	+0.18 μs
RT	200 μs	0
+80	196 μs	-0.14 μs

8.7 Because the delay line has a limited bandwidth, the rise time of the pulse increases as it progresses down the line. Since the tap coils differentiate the signal on the line, the leading edge of the output of the coils has a long slope. As the gain of the transistor changes with temperature the trigger point of the circuit also varies, thus since the slope of the output signal is finite the pulse spacing will also vary.

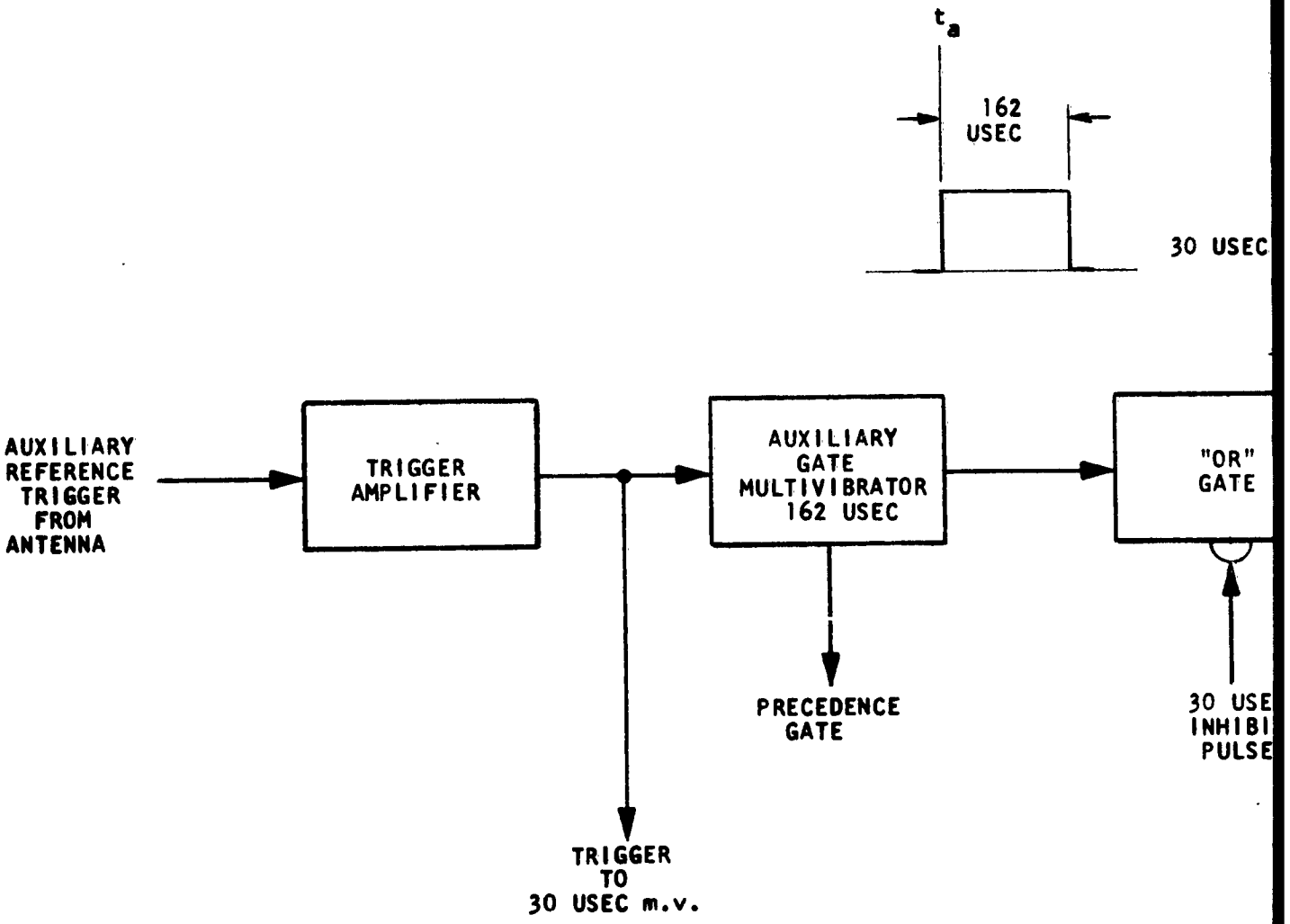

375
USEC
30 U
t_n
t_n
t_n
NORTH
REFERENCE
TRIGGER
FROM
ANTENNA
TRIGGER
AMPLIFIER
NORTH GATE
MULTIVIBRATOR
375 USEC
"OR"
PRECEDENCE
GATE
30
INH
PU
TRIGGER
TO
30 USEC MV

1

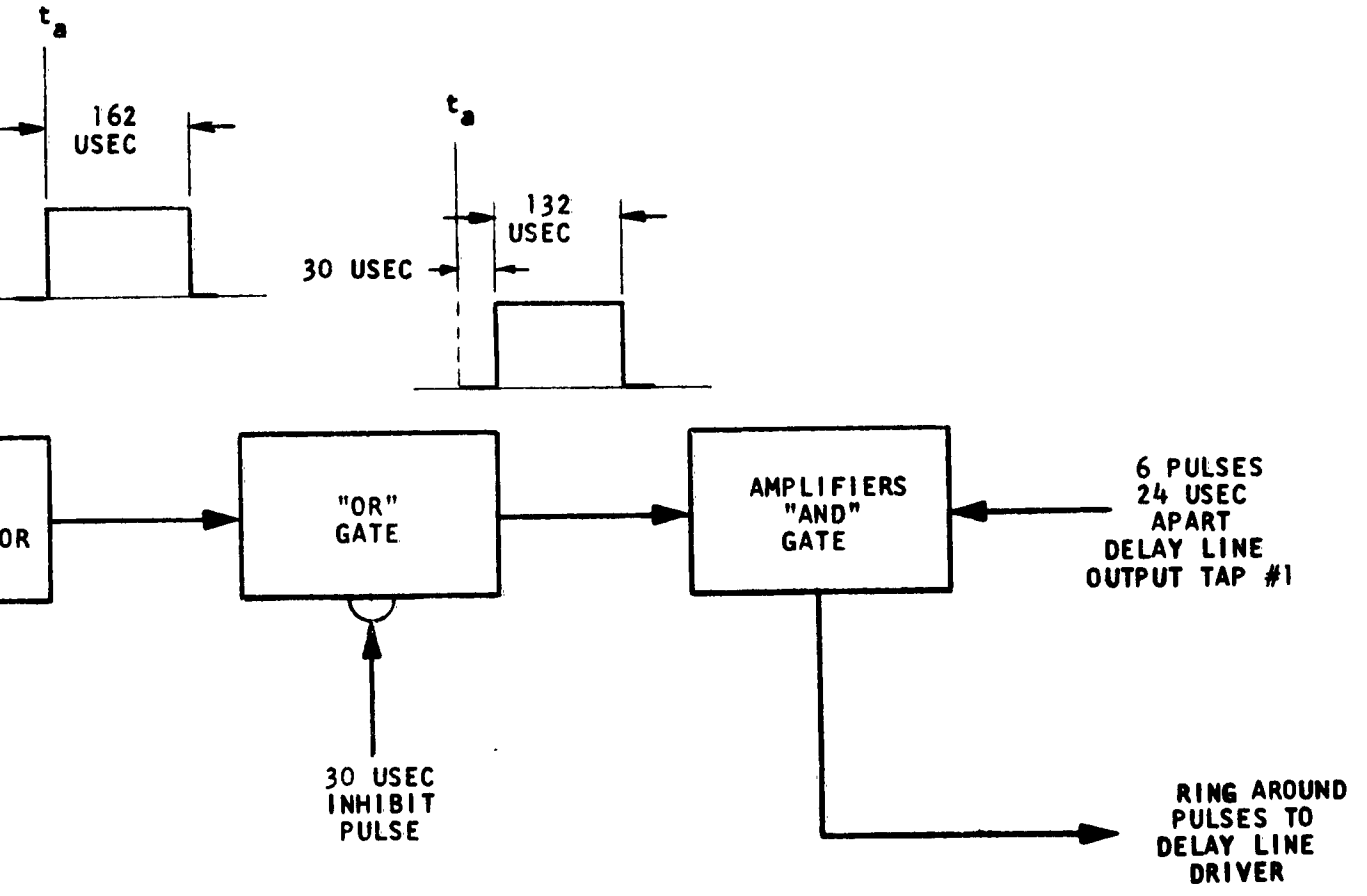


2

FIGURE 9
NORTH REFERENCE BURST
GENERATOR MODULE

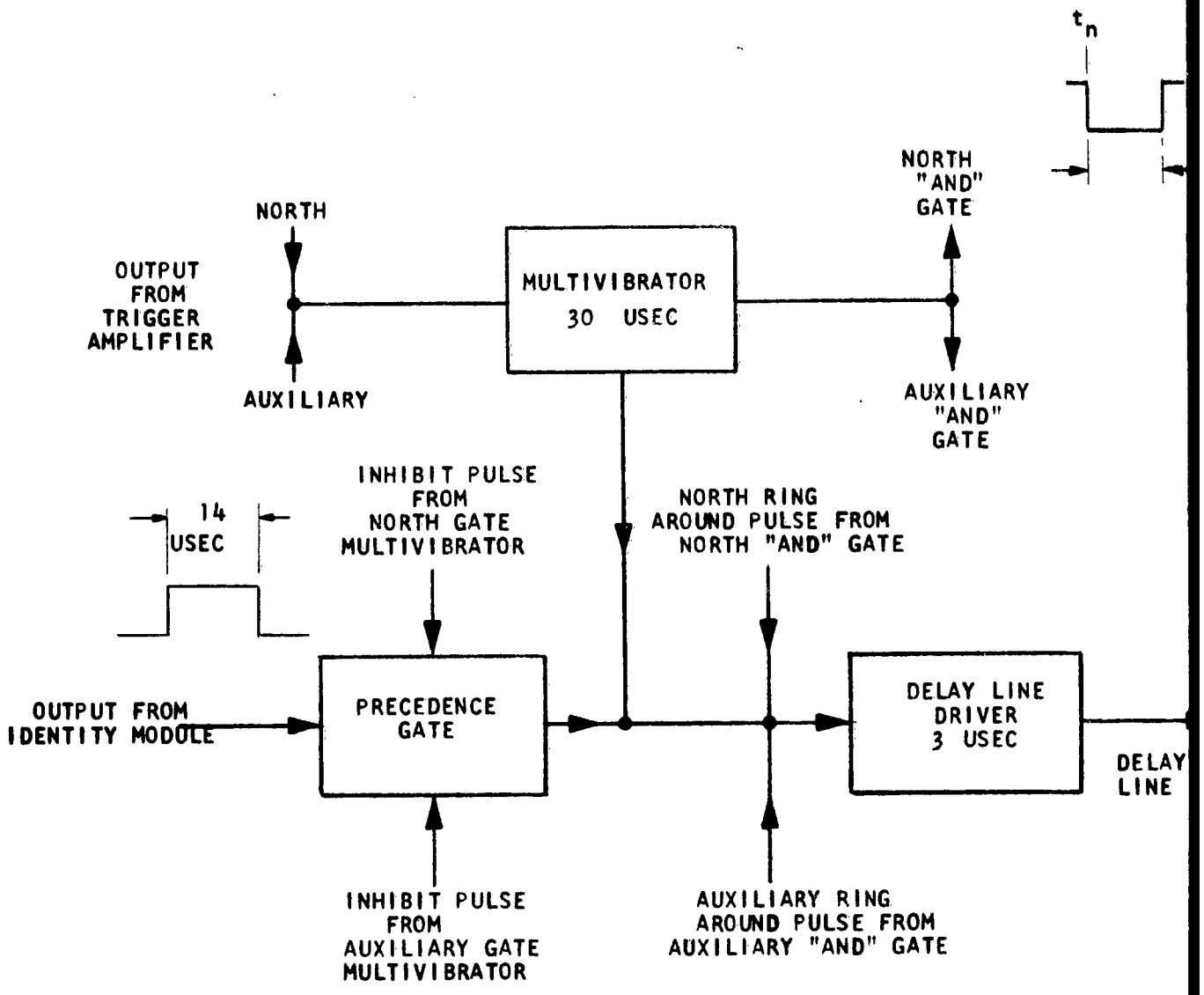

t_a
162
USEC
30 USEC
AUXILIARY
REFERENCE
TRIGGER
FROM
ANTENNA
TRIGGER
AMPLIFIER
AUXILIARY
GATE
MULTIVIBRATOR
162 USEC
"OR"
GATE
PRECEDENCE
GATE
30 USE
INHIBI
PULSE
TRIGGER
TO
30 USEC m.v.

1



2

FIGURE 10
AUXILLARY REFERENCE BURST
GENERATOR MODULE


t_n
NORTH
"AND"
GATE
NORTH
OUTPUT
FROM
TRIGGER
AMPLIFIER
MULTIVIBRATOR
30 USEC
AUXILIARY
"AND"
GATE
AUXILIARY
14
USEC
INHIBIT PULSE
FROM
NORTH GATE
MULTIVIBRATOR
NORTH RING
AROUND PULSE FROM
NORTH "AND" GATE
OUTPUT FROM
IDENTITY MODULE
PRECEDENCE
GATE
DELAY LINE
DRIVER
3 USEC
DELAY
LINE
INHIBIT PULSE
FROM
AUXILIARY GATE
MULTIVIBRATOR
AUXILIARY RING
AROUND PULSE FROM
AUXILIARY "AND" GATE

1

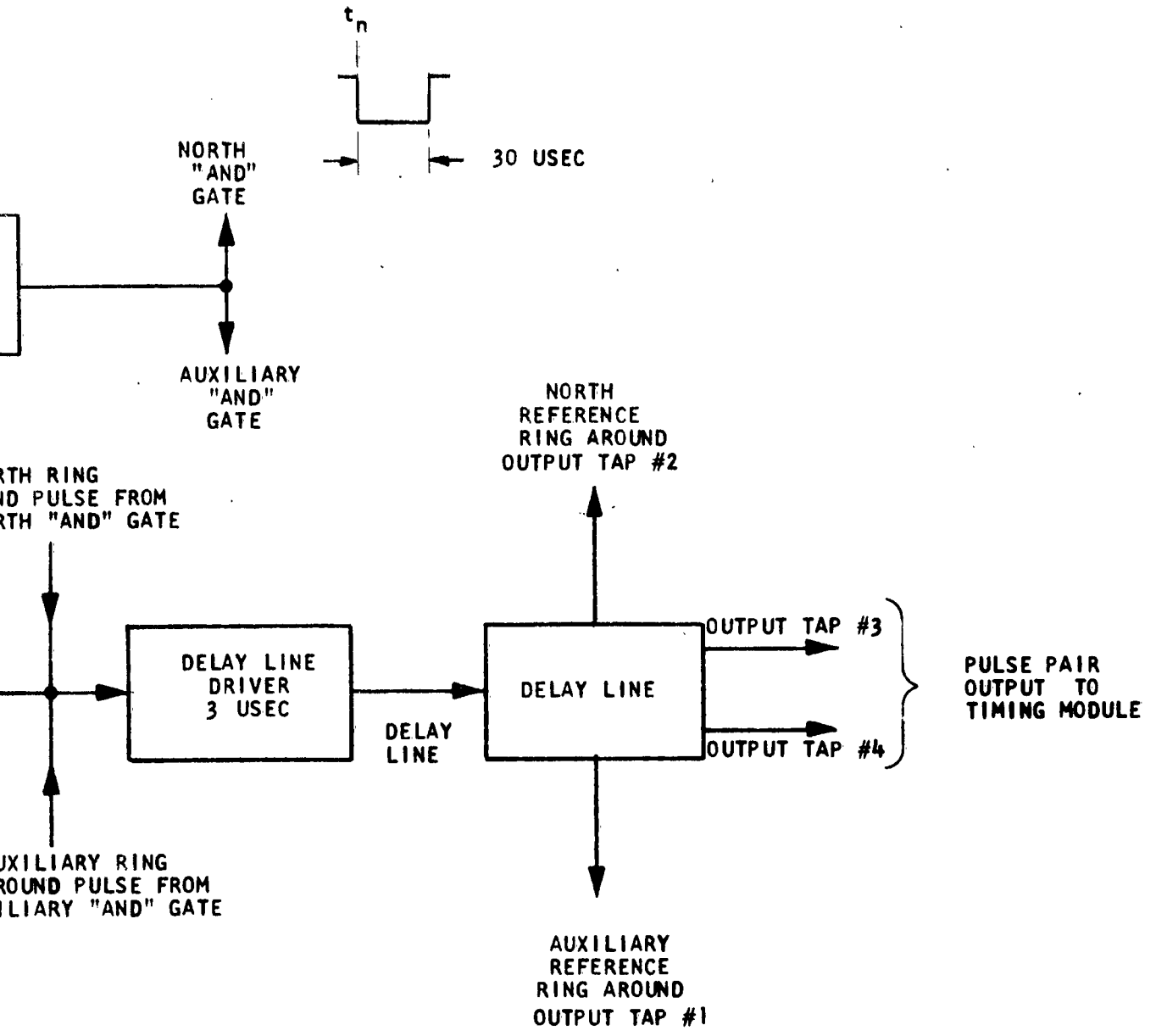


FIGURE 11
DELAY LINE DRIVER MODULE

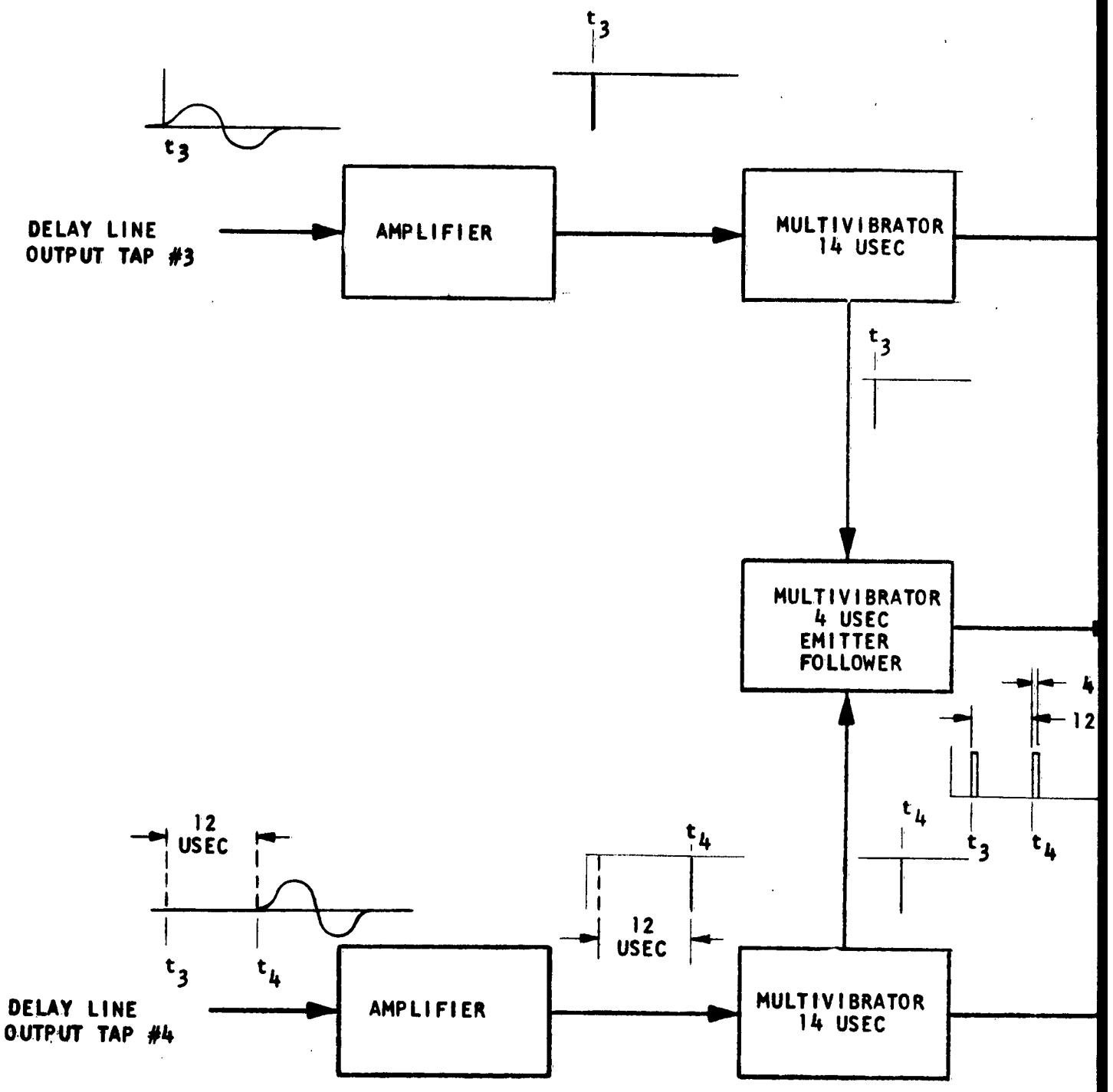
SECTION 9

TIMING MODULE (See Fig. 12)

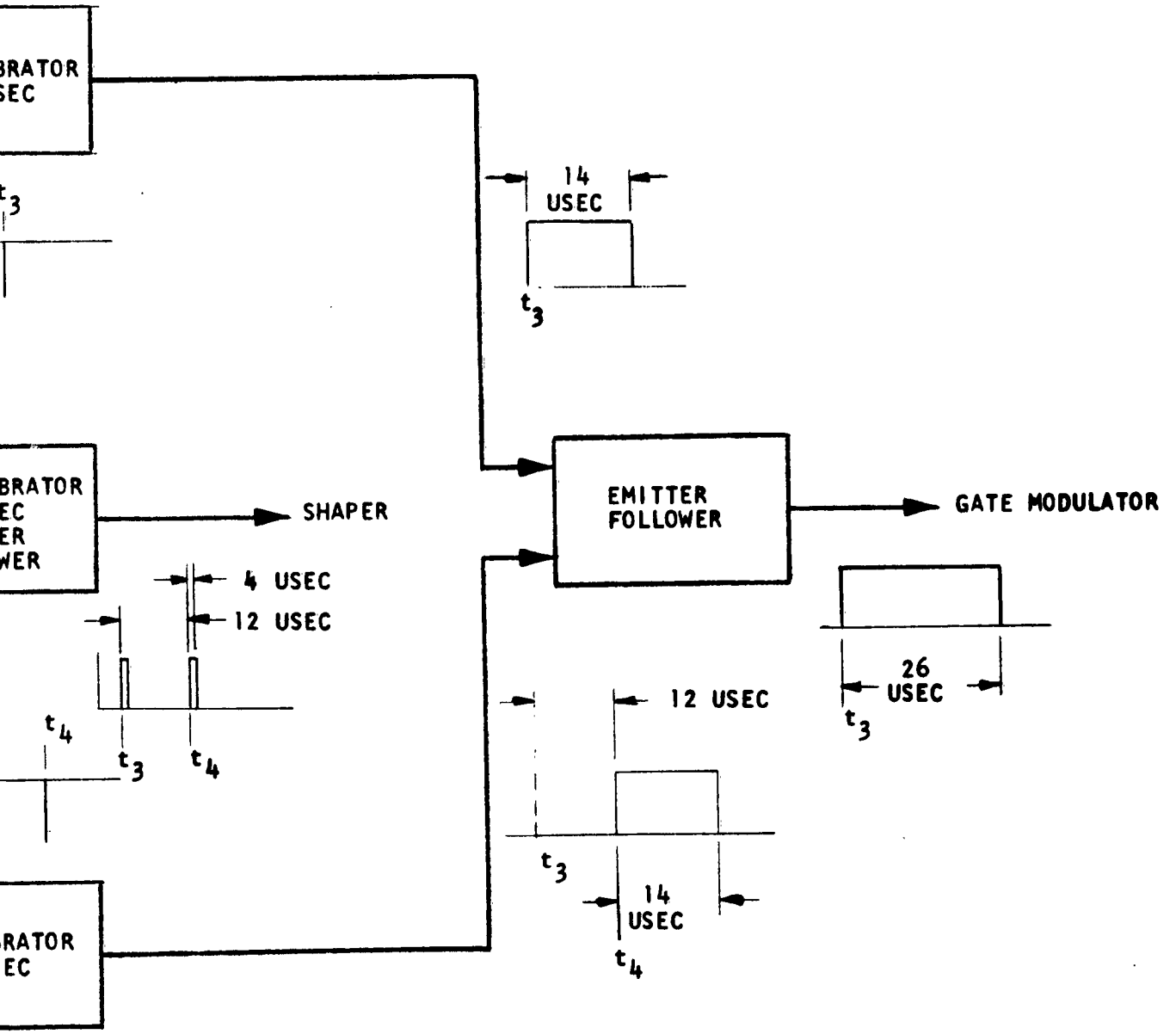
9.1 For each pulse from the bearing module, the timing module generates a pulse pair, the pulses of which are 4 μs wide and 12 μs apart, and a 26 μs pulse for blanking the receiver, and turning on the transmitter.

9.2 The third and fourth taps on the delay line are arranged so that the fourth tap adjusts the system delay, and the third, ganged to the fourth, adjusts pulse spacing. The output of each tap drives an amplifier, which in turn triggers a 14 μs multivibrator. The two 14 μs pulses, 12 μs apart, are combined by an "OR" gate to form a 26 μs pulse. The "OR" gate then feeds an emitter follower which in turn drives the gate modulator. Even though the individual, transmitted, shaped pulses have a half-amplitude width of only some 3-4 μseconds, the transmitter is gated on for 26 μs in order that the skirts of the rf output pulse will not be clipped.

9.3 The outputs of the two 14 μs multivibrators are also differentiated and used as triggers for a 4 μs multivibrator, so producing a 12 μsecond spaced pulse pair. To ensure that the first pulse of the pulse pair occurs after the leading edge of the 26 μs pulse used to gate the transmitter on, the waveform from the collector of the normally off transistor is used. The 4 μs multivibrator drives an emitter follower in order that a low source impedance is available for the filter in the shaper module.


t_3
t_3
DELAY LINE
OUTPUT TAP #3
AMPLIFIER
MULTIVIBRATOR
14 USEC
t_3
MULTIVIBRATOR
4 USEC
EMITTER
FOLLOWER
4
12
t_4
t_3
t_4
12
USEC
t_4
12
USEC
t_3
t_4
DELAY LINE
OUTPUT TAP #4
AMPLIFIER
MULTIVIBRATOR
14 USEC

1



2

FIGURE 12
TIMING MODULE

SECTION 10

SHAPER MODULE (See Fig. 13)

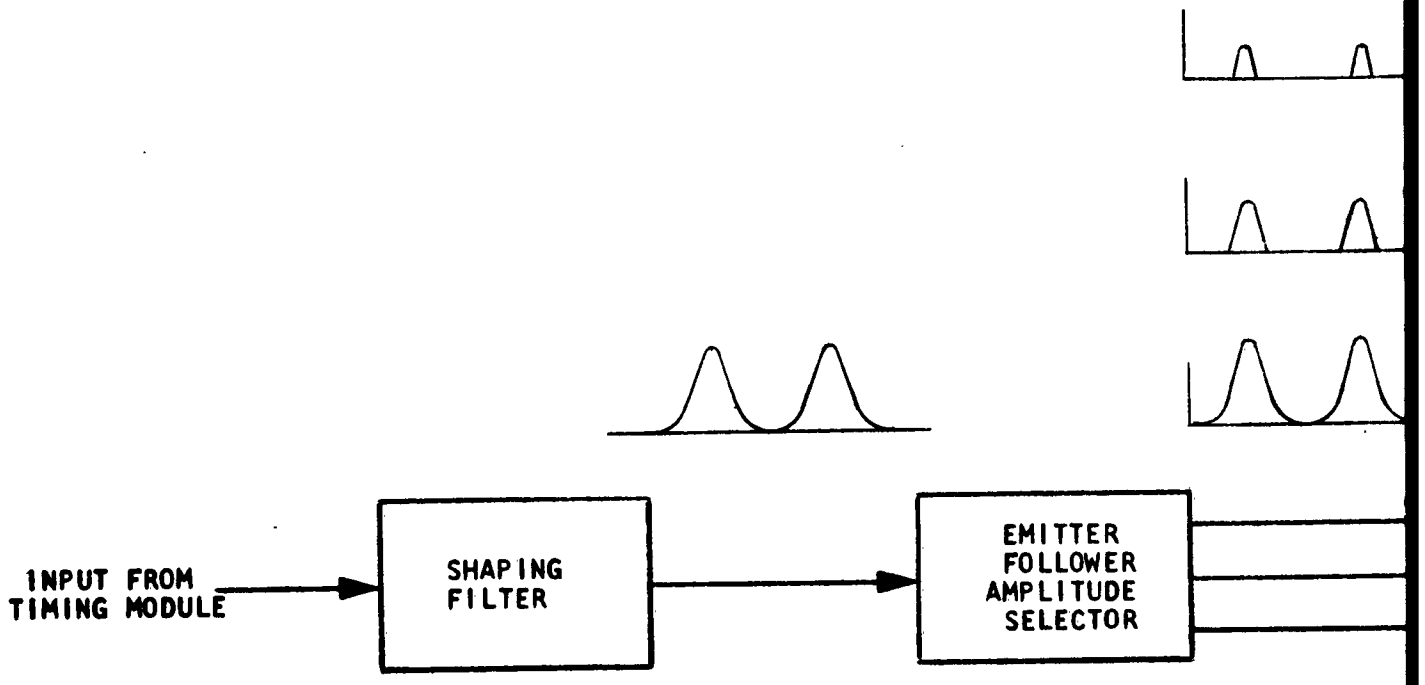
10.1 The shaper module generates the controlled waveform which it is anticipated will be required by the shaped pulse modulator in order to minimize the energy transmitted on the adjacent channel.

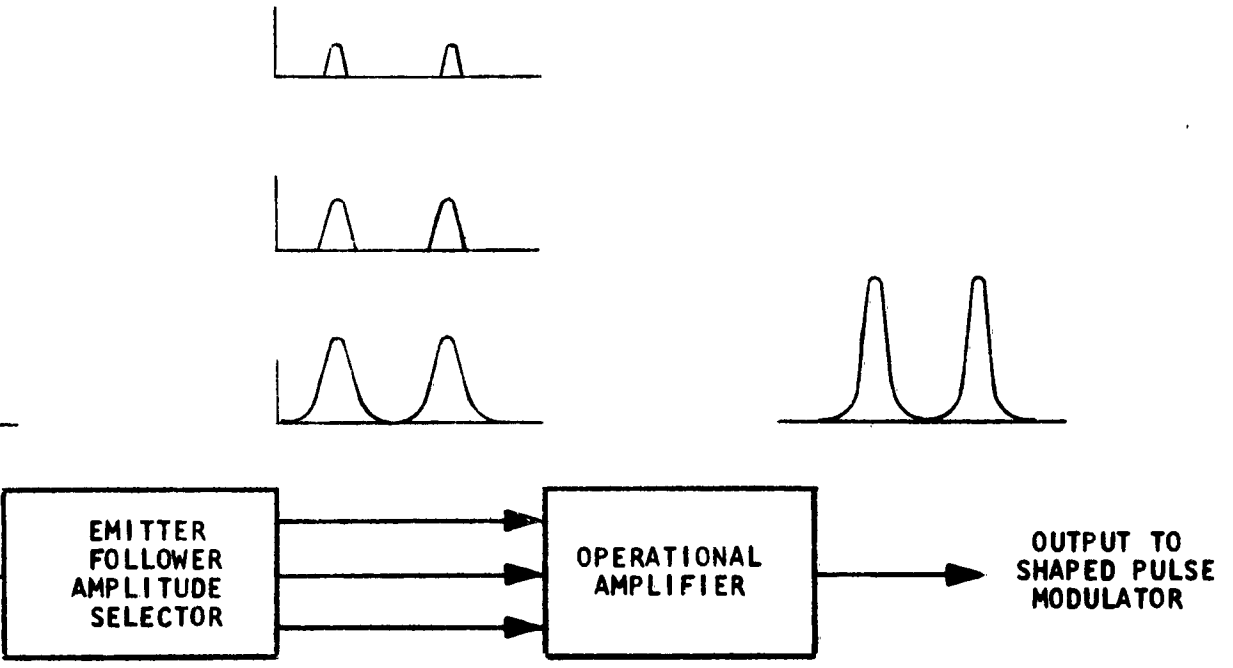
10.2 The emitter follower output stage of the timing module drives the shaper network. The latter, an 11-pole maximally flat low pass filter produces a gaussian-like output pulse when driven from a voltage source.

10.3 Initially, a technique using a single LC ringing circuit to develop a sine-squared waveform which in turn could be modified by slicing techniques was used. This yielded poor results because of the long recovery time associated with such an arrangement. Satisfactory results were obtained with separate multivibrator, emitter-follower, LC ringing chains for each of the pulses in the pulse pair, however the resulting circuit complexity discouraged any further investigations in this area. The low-pass filter technique, although requiring a more complex tuning procedure has resulted in the best performance, especially with regard to droop and amplitude variations in the reference bursts. Amplitude variations of less than ±0.5%, and reference burst doop of the same magnitude were obtained at the filter output.

10.4 Since the transfer characteristic of the shaped pulse modulator and transmitter is highly non-linear, the shaped pulse must be predistorted. This is accomplished by the amplitude selector, using a sampling and slicing technique. The peak and skirts of the output pulse can be independently adjusted and the desired shape obtained.

10.5 The sampled outputs of the amplitude selector are combined in an operational amplifier. (See appendix no. 2 for a derivation of the voltage gain equation of this amplifier). This particular configuration was selected because the virtual ground resulting at the base of the input transistor minimizes interaction among the several inputs. The large amount of negative feedback employed results in an amplifier whose voltage gain is virtually independent of variations in transistor parameters.


INPUT FROM
TIMING MODULE
SHAPING
FILTER
EMITTER
FOLLOWER
AMPLITUDE
SELECTOR



2

FIGURE 13
SHAPER MODULE

SECTION 11

SUMMARY AND RECOMMENDATIONS

11.1 On the basis of the work we have done to date on this contract it is evident that a solid-state TACAN receiver-coder is no longer state-of-the-art. The techniques on which the development is based have been thoroughly explored, and an operating breadboard constructed which shows considerable promise. With this background it would appear desirable that the contractor be permitted to continue development to the point where a fully-packaged unit is available, capable of operation over a full -40°C to +80°C temperature range without readjustment.

11.2 While the receiver-coder and monitor development contracts awarded to ITTFL by the USAF have stimulated development to the point where advanced prototype models can now be constructed, serious gaps exist in the program. To our knowledge no transmitter or test equipment has been developed suitable for accompanying the receiver-coder and monitor, although valuable work towards a solid-state transfer and control unit has been started in the add-on to the original monitor contract. As the scientific report for the monitor contract covers the transfer/control and test equipment recommendations, the rest of the summary will be restricted to the transponder.

11.3 With the background this laboratory has received in USAF requirements with the AN/TRN-17 and solid-state TACAN R and D contracts, it appears that three broad types of TACAN/DMET transponders may be desirable to meet all USAF applications. First, an ultra-lightweight low-power transponder suitable for use as a marker beacon, which could be air-droppable and capable of being lifted by a man. Second, a mobile system with the facilities of the AN/TRN-17 but of considerably reduced size, weight, and power consumption. Third, a high-power system of improved performance over the GRN-9 series beacon for fixed applications. An 8" x 8-1/2" x 15" solid-state receiver-coder forms the ideal basis for a comprehensive modular approach to meeting all these requirements.

11.4 The transmitter for the first and second applications can be readily met by a further development of the driver amplifier developed for the AN/TRN-17. This unit can be made continuously tunable over both bands, and with duplexer, solid-state multiplier and modulators could be packaged in a further 8" x 8-1/2" x 15" module to provide 400-500 watts peak with a 45-50 db spectrum. The size of these two basic building blocks, it is believed, meets the basic requirements for the first USAF requirement (See Par. 10.3), and due to the output power available these same two building blocks could be masthead mounted to meet the second USAF requirement. This would be fully practicable from the viewpoint of weight, size and reliability,

and indeed would produce a radiated power in excess of that provided by the NA/TRN-17 due to the absence of antenna feeder cable losses. Supplies, test and monitor equipment would of course be still shelter-mounted, and facilities provided to lower the inactive transponder to the ground for routine maintenance.

11.5 In the third area of USAF requirements, that of high-power fixed systems, it would appear that no output tube superior to the Sperry SAL-219 klystron is yet available for the generation of 10KW, 60 db spectrum, TACAN signals. Again, however, the same receiver-coder, multiplier and driver amplifier can be used.

11.6 Summarizing, this contractor would recommend the following:

a) That the USAF support the further development of the receiver-coder developed under contract AF19(604)-8352 to the point where it is capable of full -40°C to +80°C operation and is fully packaged.

b) That the USAF consider the packaged receiver-coder as a basic building-block on which to base a comprehensive modular approach, for meeting its different operational requirements for TACAN transponders with complete interchangeability.

APPENDIX I

APPENDIX I

DESIGN OF THE INTER-STAGE COUPLING NETWORKS

1. The design approach is essentially that of Rexroad (2)*, using equations from Valley and Wallman (3)*

f_o, the midband frequency

$W_o = 2\pi f_o = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$

$k = \frac{M}{L_1 L_2}$, the coefficient of coupling

$s = K Q_1 Q_2$, the coupling index

BW, the 3 db stage bandwidth

$v = Q_1 Q_2 \left(\frac{W}{W_o} - \frac{W_o}{W}\right)$, the frequency variable

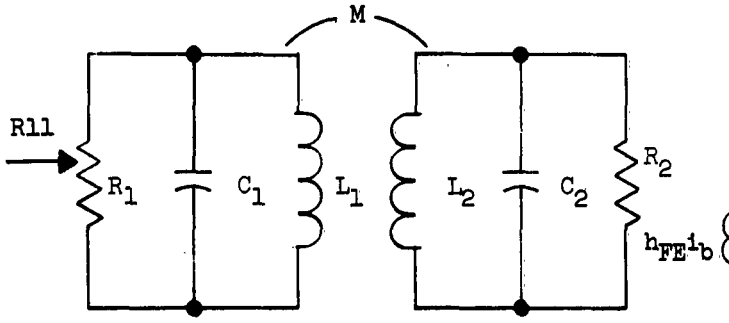


Figure A-1
Basic Double-Tuned Circuit

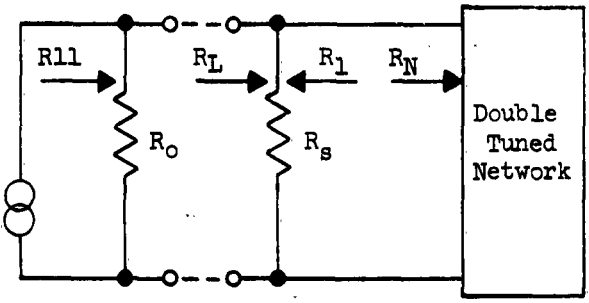


Figure A-2
Load Presented to the Transistor

* See List of References

R_{11}, driving point resistance of entire network

R_o, output resistance of the transistor under the desired operating conditions.

R_1, input resistance of the transistor under the desired operating conditions.

R_s, swamping resistance used across L_1.

R_N, input resistance of the coupled double-tuned network.

R_L, load presented to the transistor, R_s in parallel with R_N.

$M_m = \frac{R_o}{R_L}$, the mismatch ratio

From Figure A-2 and the definition of mismatch above

$$R_L = \frac{R_s R_N}{R_s + R_N} = \frac{R_o}{M_m} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

which when solved for R_n, gives

$$R_N = \frac{R_o R_s}{M_m R_s - R_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Substituting R_o = 7,000 ohms from the average value measured on the sample 3N35's, and M_m = 5 as the desired amount of mismatch

$$R_N = \frac{(7,000)\ R_s}{5R_s - 7000}$$

By choosing $R_s = 1.5\ R_N$

$$R_N = \frac{(7,000)\ (1.5R_N)}{(5)(1.5R_N) - 7000} = 2,330 \text{ ohms}$$

and R_s = 1.5 (2,330) = 3500 ohms (use 3,300 ohms)

From Figure 2A, R_1 is the parallel combination of R_o and R_s

$$R_1 = \frac{R_o R_s}{R_s + R_N} = \frac{(7,000)(3,300)}{7,000+3,300} = 2,250 \text{ ohms} \quad \ldots\ldots\ldots\ldots (3)$$

and R_L the parallel combination of R_s and R_N

$$R_L = \frac{R_s R_N}{R_s + R_N} = \frac{(3,300)(2,330)}{3,300+2,330} = 1,370 \text{ ohms} \quad \ldots\ldots\ldots\ldots (4)$$

The driving point resistance R_{11} of Figure A-2 is

$$R_{11} = \frac{R_o R_L}{R_o + R_L} = \frac{R_o \left(\frac{R_o}{M_m}\right)}{R_o + \frac{R_o}{M_m}} = \frac{R_o}{M_m + 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The driving point admittance, $G_{11} = \frac{1}{R_{11}}$ has been expressed by

Valley and Wallman as

$$G_{11} = \frac{1}{R_{11}} = \frac{1}{R_1} + \frac{S^2}{R_1 \left(1 + \frac{Q_2 \gamma^2}{Q_1}\right)} \quad \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

substituting γ = o at W = Wo gives

$$R_{11} = \frac{R_1}{S^2 + 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

equating (7) to (5)

$$\frac{R_1}{S^2+1} = \frac{R_o}{M_m+1}$$

$$\text{or } R_1 = \frac{R_o (S^2 + 1)}{M_m + 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

For critical coupling S = 1 and R1 equals

$$R_1 = \frac{2R_o}{\frac{M}{m}+1} = \frac{2(7,000)}{5+1} = 2,330 \text{ ohms} \quad \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

verifying that $R_1 = R_n$ for critical coupling

The primary tuned circuit may be represented by Figure A-3

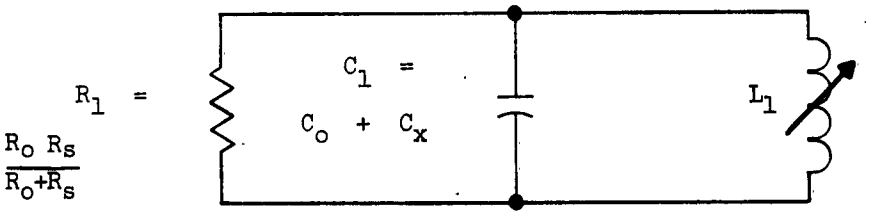


Figure A-3

Primary Tank Circuit

The 3 db bandwidth for transitional coupling is

$$BW = \sqrt{\frac{1 + k^2 Q_1 Q_2 f_o}{Q_1 Q_2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

which reduces to

$$BW = \frac{\sqrt{2} f_o}{Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (11)$$

for the case where $Q_1 = Q_2 = Q$, S = 1, the coefficient of coupling k is given by

$$k = \frac{S}{\sqrt{Q_1 Q_2}} = \frac{1}{Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

At an expected gain of 12 db per stage the bandwidth shrinkage factor is applied for ten stages.

$$BW = \frac{BW\ tot.}{\sqrt[4]{2^{1/n} - 1}} = \frac{3MC}{\sqrt[4]{2^{1/10} - 1}} = 5.8\ MC \quad \ldots\ldots\ldots\ldots (13)$$

which when substituted into equation (11) yields

$$Q = \frac{\sqrt{2}\ (63)}{5.8} = 15.5 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (14)$$

C_1 is found from the definition

$$C_1 = \frac{Q}{W_o R_1} = \frac{15.5}{(3.9 \times 10^8)\ (2,250)} = 17.7\ pf \quad \ldots\ldots\ldots\ldots (15)$$

Since this value represents the transistor output capacity, measured at 2.5 pf, in parallel with a required external capacity C_x, the value used is

$$C_x = C_1 - C_o = 17.7 - 2.5 = 15.2\ pf\ (use\ 15\ pf) \quad \ldots\ldots\ldots (16)$$

As the coils will be tunable the nominal primary inductance is

$$L_1 = \frac{1}{W_o^2 C_1} = \frac{1}{(3.9 \times 10^8)^2 (17.7 \times 10^{-12})} = 0.36\ \mu h \quad \ldots\ldots\ldots (17)$$

The low input resistance, $R_i = 120$ ohms, seen at the transistor input would require a secondary circuit capacity in the order of 330 pf, which is not practical. The approach, therefore, is to assume a reasonable value of capacity and step up the input resistance seen across the coil by means of a capacitor divider (see Figure A-4).

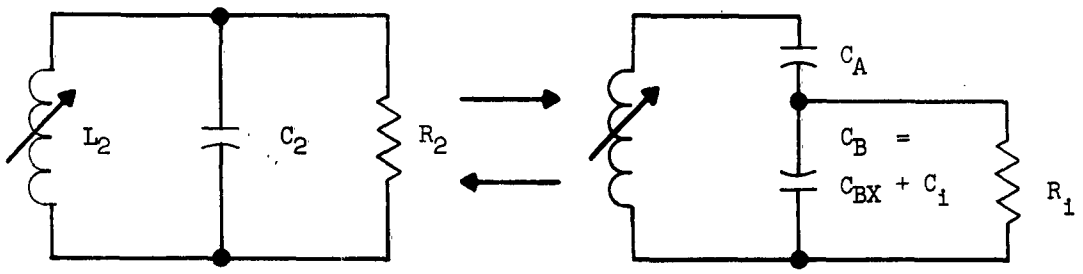


Figure A-4

Secondary Tank Circuit

Assume C_2 = 25 pf, then the required resistance to appear across L_2 is

$$R_2 = \frac{Q}{W_o C_2} = \frac{15.5}{(3.9 \times 10^8)(25 \times 10^{-12})} = 1{,}400 \text{ ohms} \quad \ldots\ldots\ldots (18)$$

This resistance is R_i transferred through the capacitive divider as follows

$$R_2 = R_i N^2 = R_i \left(\frac{C_A+C_B}{C_A}\right)^2$$

$$\text{or } \left(\frac{C_A+C_B}{C_A}\right)^2 = \frac{R_2}{R_i} = \frac{1400}{120} = 13.2 \quad \ldots\ldots\ldots\ldots\ldots\ldots (19)$$

Knowing that

$$\frac{C_A C_B}{C_A+C_B} = C_2 = 25 \text{ pf} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (20)$$

Equations (19) and (20) are solved simultaneously for C_A and C_B giving C_A = 39 pf and C_B = 95 pf

where C_B less the parallel transistor input capacity of 30 pf is the required external base shunting capacitor C_{XB}.

$$C_{XB} = C_B - C_i = 95\text{-}30 = 65 \text{ pf} \quad \ldots\ldots\ldots\ldots\ldots (21)$$

The coefficient of coupling for the equal Q transitionally coupled case is given by equation (12) as

$$k = \frac{1}{Q} = \frac{1}{15.5} = 0.065 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (22)$$

2. Transistor D-C Operation

2.1 For optimum gain characteristics, the manufacturer suggests an operating point of $V_{oE} = 20$, $I_E = 1.3$ ma, and $I_{B2} = -100$ μa. To ensure adequate bias circuit performance from unit to unit under conditions of large ambient temperature variations, a symmetrical plus and minus 25.2 volt arrangement is used, (see Figure A-5).

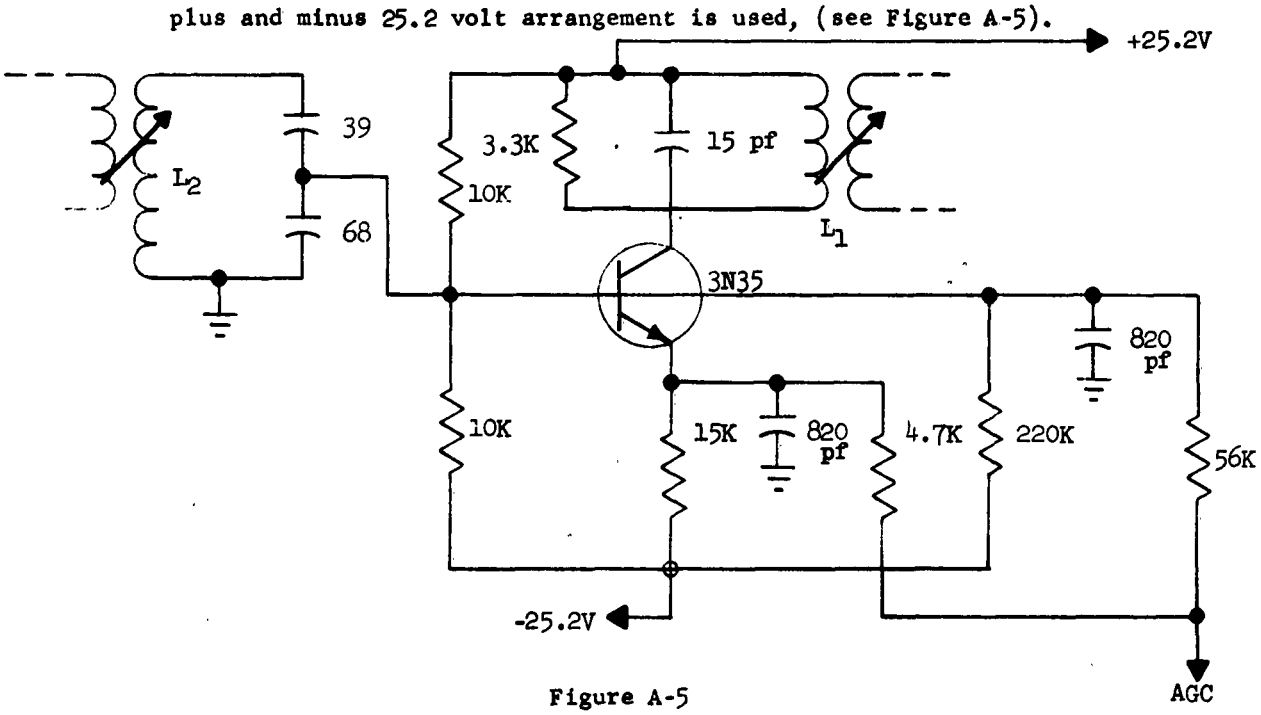


Figure A-5

One Stage of I.F. Amplifier

The equal resistance base bias divider provides a DC return for the base while holding it at approximately zero volts. All values of R_{iep}, C_{iep}, R_{oep}, C_{oep}, used in previous calculations are based on this operating point.

2.2 From the published data on the 3N35 and the chosen operating point, the upper operating temperature limit was found as follows:

2.3 The maximum allowable collector dissipation of the 3N35 is 125 mW at 25°C, derated 1 mW/°C.

$$T_{max.} = 25°C + (P_{MAX} - V_{CE} \times I_C)\ mW \times 1\ \frac{°C}{mW}$$

$$= 25 + (125 - 25 \times 1.3) \times 1$$

$$T_{max.} = 117.5°C$$

2.4 Since 80°C is the upper temperature limit at which the IF Amplifier is expected to operate there is no danger of over-dissipation.

3. Temperature Stability

3.1 The variation in collector current with temperature depends on the three variables I_{co}, V_{BE}, and h_{FE} which can be represented by their stability factors S1, S2, and S3 respectively. The changes in I_{co}, V_{BE}, and h_{FE}, as calculated from the normalized 3N35 data sheet curves are tabulated (Table A-1) over a temperature range of -40°C to +80°C.

Table A-1

3N35 TEMPERATURE VARIATIONS

Temp (°C)	-40	+25	+80
I_{co} (μa)	0.0006	0.02	0.25
V_{BE}* (volts)	0.431	0.6	0.743
h_{FE}	21.2	2.5	23.7

* Decreases 2.6 mV/$^{o}_{C}$

Equations used for the following calculations are those derived in Hunter (3)*.

$$S_1 = \frac{\Delta I_c}{\Delta I_{co}} = (h_{FE} + 1) \times \frac{1 + \frac{R_B}{R_E}}{(h_{FE}+1) + \frac{R_B}{R_E}} = 1.18$$

$$S_2 = \frac{I_c}{V_{BE}} = \left(\frac{1}{R_E}\right) \times \frac{h_{FE}}{(h_{FE}+1) + \frac{R_B}{R_E}} = -4 \text{ millimhos}$$

$$S_3 = \frac{I_c}{h_{FE}} = \frac{S_1 \; I_{c1}}{h_{FE1}(h_{FE2}+1)} = 3.18 \times 10^{-3} \text{ma at } -40°C \text{ \& } 2.84 \times 10^{-3} \text{ma at } +80°C$$

The total change in collector current is the sum of the individual changes as follows:

$$\Delta I_c = S_1 \, \Delta \, I_{co} + S_2 \, \Delta \, V_{BE} = S_3 \, \Delta \, h_{FE}$$

at -40°C

$$\Delta I_c \text{ (in ma)} = (1.18)(-0.02\times10^{-3}) + (-4\times10^{-3})(0.169) + (3.18\times10^{-3})(-3.8)$$

thus $I_c = -0.013$ ma at -40°C

at +80°C

$$\Delta I_c \text{ (in ma)} = (1.18)(0.23\times10^{-3}) + (-4\times10^{-3})(-0.143) + (2.84\times10^{-3})(-1.3)$$

thus $\Delta I_c = -0.003$ ma at +80°C

Summarizing, ΔI_c (TOT.) = -0.010 ma

ΔI_c (TOT.) is sufficiently small in terms of the normal quiescent collector current of 1.6 ma, to consider the circuit bias stable.

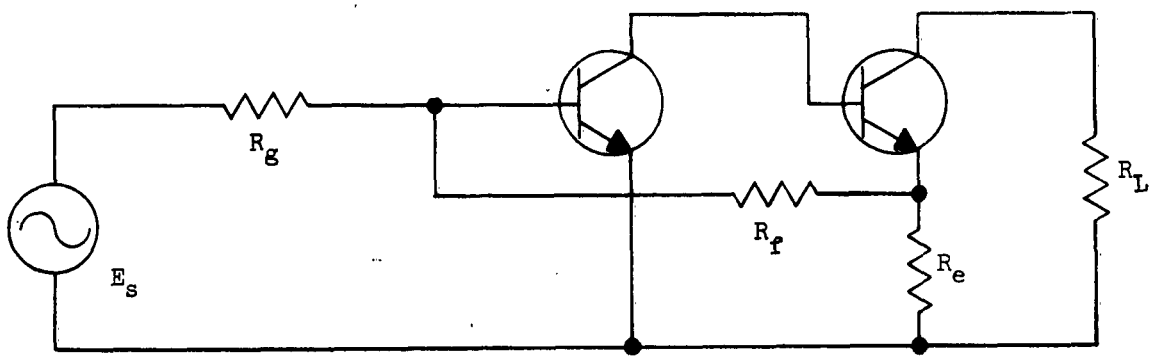
* See List of References.

APPENDIX II

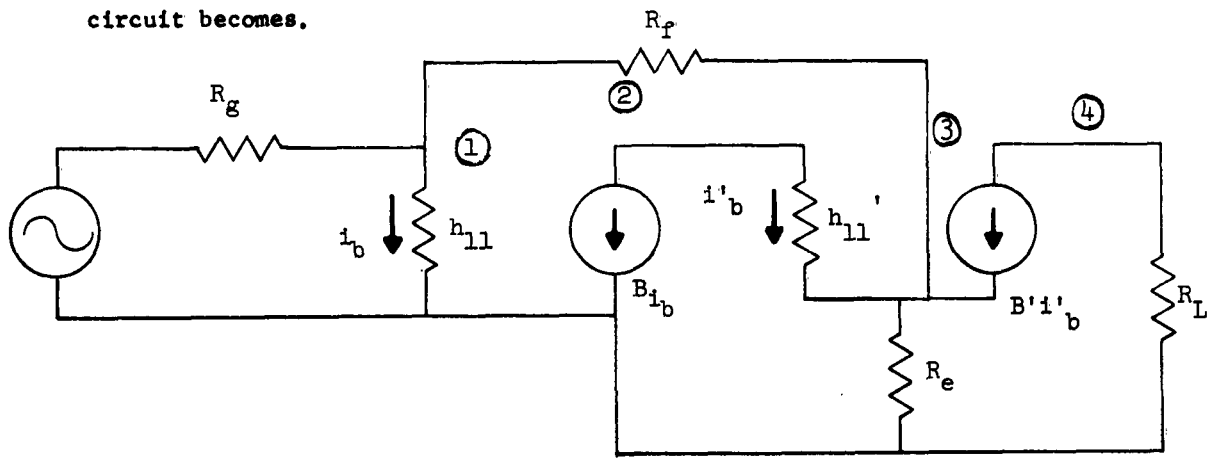
APPENDIX II

DERIVATION OF GAIN EQUATION FOR THE FEEDBACK AMPLIFIER PAIR

1. The decoder and shaping module use a two stage amplifier with feedback from the emitter of the second stage to the base of the first stage. The simplified circuit neglecting the effects of the bias resistors is shown below.



2. Replacing the transistors with equivalent h parameters the circuit becomes.



3. The equivalent circuit neglects the leakage current which is less than a micro-amp in a silicon unit and the output admittance which is typically about 10^{-5} mhos. Nodal analysis of the above circuit at the points numbered yields the following equations.

$$E_1 (Y_g + Y_{11} + Y_f) - E_3 Y_f = E_s Y_g = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$E_1 B Y_{11} + E_2 Y_{11}' - E_3 Y_{11}' = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

$$E_1 Y_f - E_2 (1 + B_2) Y_{11}' + E_3 \left[(1 + B') Y_{11}' + Y_{RE} = Y_f\right] = 0 \quad \ldots \quad (3)$$

$$E_2 Y_{11}' B' - E_3 B' Y_{11}' + E_4 Y_{11} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

4. The gain of the amplifier can be determined by solving for E_4 using Cramer's rule

$$K = \frac{E_4}{E_S} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

$$= \frac{R_L}{\left[\left(\frac{B' + 1}{B'}\right)\left(\frac{Y_f}{Y_g (Y_e + Y_f)}\right)\right] - \left[\frac{Y_f^2}{B' B (Y_e + Y_f) Y_g Y_{11}}\right] + \left[\frac{Y_g + Y_{11} + Y_f}{B' B Y_{11} Y_g}\right]}$$

5. Since the minimum beta of both the 2N338 (first stage) and the 2N699 (second stage) is 45, the second and third terms of the denominator of the gain equation can be considered negligible. These terms can be calculated using typical values.

	2N338	2N699
B	45	45
h_{11}	2^k	2^k

* $Y_f = 0.2 \times 10^{-3}$ mho

* $Y_g = 0.5 \times 10^{-4}$ mho

* $Y_e = 1 \times 10^{-3}$ mho

* values used in the operational amplifier

The first term at the denominator of equation (5) is = 3.25×10^3 ohms

The second term at the denominator of equation (5) is = 1.93 ohms

The third term at the denominator of equation (5) is = 61.7 ohms

6. The gain is thus dependent only on fluctuations in the alpha of the second stage and the circuit components. Even though the beta of the transistor may change by 50% with changes in temperature, alpha will only vary by 3%. Since alpha is very close to unity the approximate gain of the amplifier is given by the following equation.

$$K = \frac{(R_e + R_f)\, R_L}{R_e\, R_g} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

E_s = source voltage

R_g = source resistance

R_f = feedback resistance

R_e = emitter resistance

R_L = load resistance

h_{11} = transistor input impedance

i_b = transistor base current

B = transistor current gain

K = voltage gain of the amplifier

REFERENCES

1. Pritchard, R.O., "High Frequency Power Gain of Junction Transistors", Proc. IRE, Vol. 43, September 1955, pp. 1075-1085

2. Rexroad, W.D., "Get Stability Through Mismatching", Electronics, McGraw-Hill Publications, October 19, 1962, pp. 50-53

3. Valley, G.E., and Wallman, H., "Vacuum Tube Amplifiers", Radiation Laboratory Series, Vol. 18, Chapter 5, 1948.

4. Hunter, L.P., "Handbook of Semiconductor Electronics", McGraw-Hill Book Company, New York, 1962

5. Beneteau, P.J., "The Design of High Stability D.C. Amplifiers", Fairchild Semiconductor App. 23/2

Electronic Systems Division L. G. Hanscom Field, Bedford, Mass.
ESD-TDR-63-128 SOLID STATE TACAN RECEIVER CODER Mar. 63 43 p.
Unclassified Report

The initial design of a receiver coder for use as part of a solid state TACAN ground system is discussed. Techniques developed for specific problem areas are covered; and experimental results obtained from a 'breadboard' model given. The possible implications of the program on future TACAN developments are examined and recommendations made for the future course of development.

1. Radio Beacons
2. Solid State Physics
3. Experimental Data, Design

I Contract AF19(604)-8352
II ITT Federal Labs Nutley, N. J.
III In ASTIA collection

Electronic Systems Division L. G. Hanscom Field, Bedford, Mass.
ESD-TDR-63-128 SOLID STATE TACAN RECEIVER CODER Mar. 63 43 p.
Unclassified Report

The initial design of a receiver coder for use as part of a solid state TACAN ground system is discussed. Techniques developed for specific problem areas are covered; and experimental results obtained from a 'breadboard' model given. The possible implications of the program on future TACAN developments are examined and recommendations made for the future course of development.

1. Radio Beacons
2. Solid State Physics
3. Experimental Data, Design

I Contract AF19(604)-8352
II ITT Federal Labs Nutley, N. J.
III In ASTIA collection

Electronic Systems Division L. G. Hanscom Field, Bedford, Mass.
ESD-TDR-63-128 SOLID STATE TACAN RECEIVER CODER Mar. 63 43 p.
Unclassified Report

The initial design of a receiver coder for use as part of a solid state TACAN ground system is discussed. Techniques developed for specific problem areas are covered; and experimental results obtained from a 'breadboard' model given. The possible implications of the program on future TACAN developments are examined and recommendations made for the future course of development.

1. Radio Beacons
2. Solid State Physics
3. Experimental Data, Design

I Contract AF19(604)-8352
II ITT Federal Labs Nutley, N. J.
III In ASTIA collection

Electronic Systems Division L. G. Hanscom Field, Bedford, Mass.
ESD-TDR-63-128 SOLID STATE TACAN RECEIVER CODER Mar. 63 43 p.
Unclassified Report

The initial design of a receiver coder for use as part of a solid state TACAN ground system is discussed. Techniques developed for specific problem areas are covered; and experimental results obtained from a 'breadboard' model given. The possible implications of the program on future TACAN developments are examined and recommendations made for the future course of development.

1. Radio Beacons
2. Solid State Physics
3. Experimental Data, Design

I Contract AF19(604)-8352
II ITT Federal Labs Nutley, N. J.
III In ASTIA collection